Bubble Memory Design Handbook

one megabit

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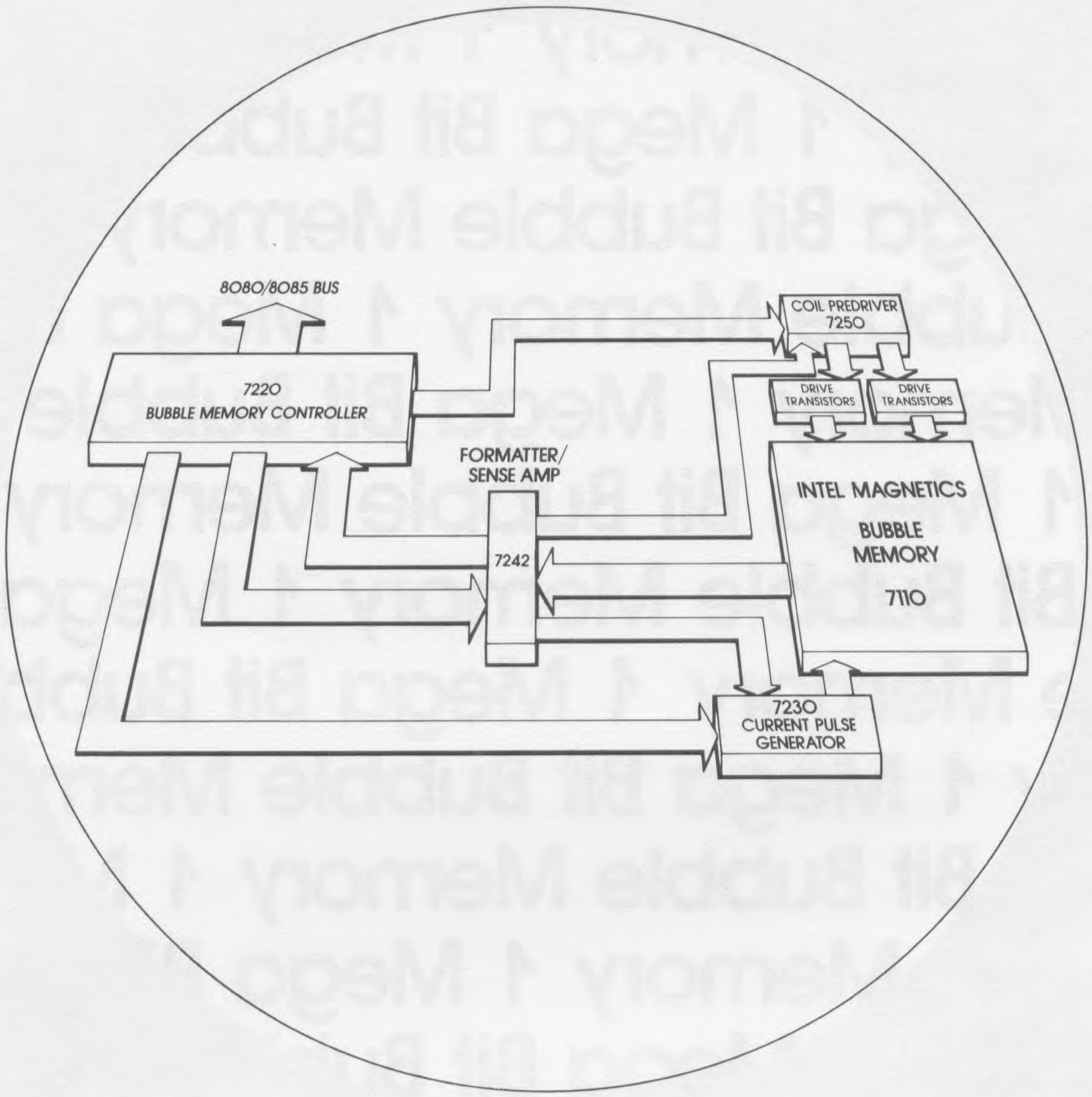
Bubble Memory Design Handbook



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Bubble Memory Design Handbook

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Preliminary

7110, 7112
1 MEGA BIT BUBBLE MEMORY

Features

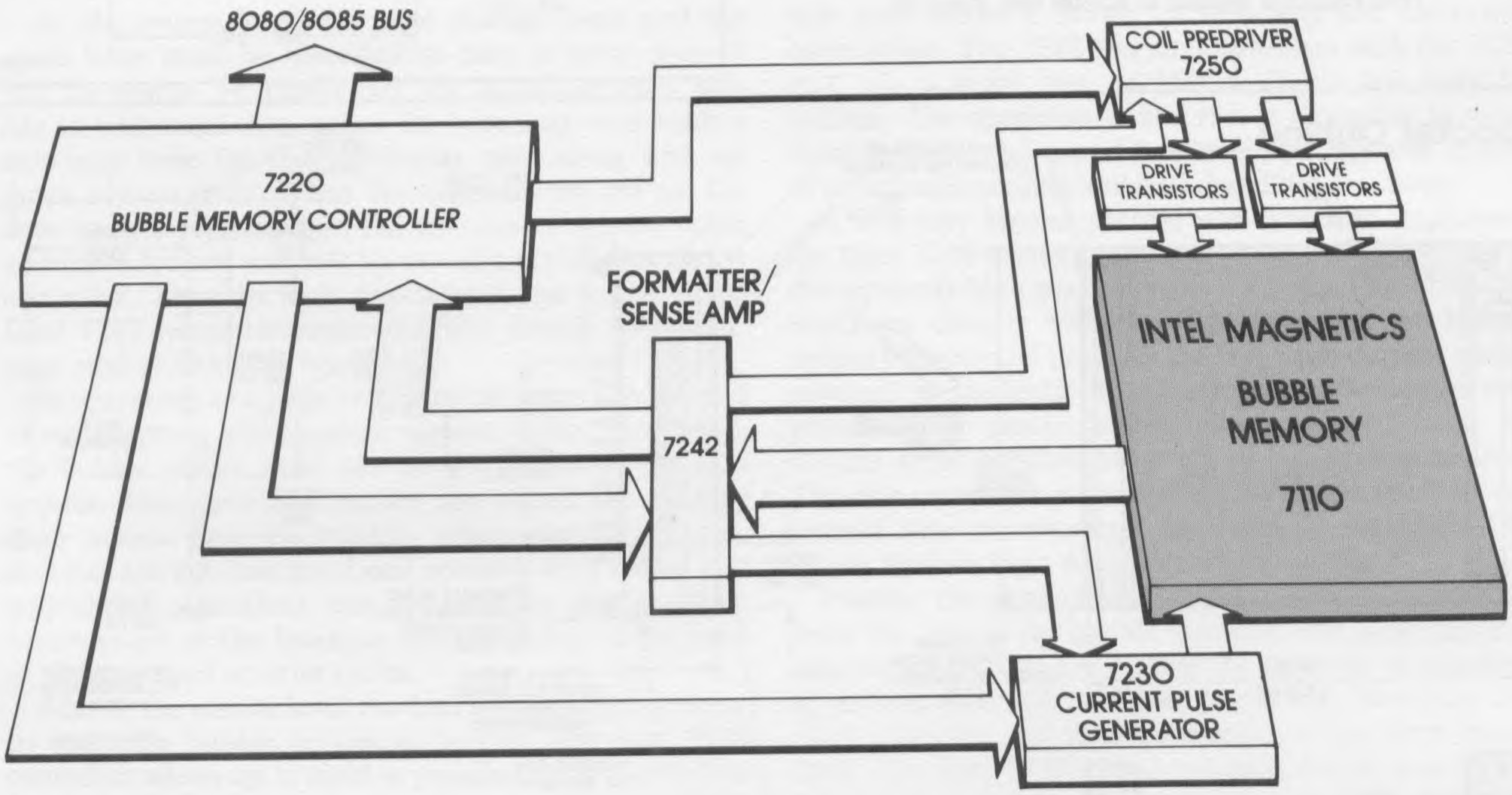
- 1,048,576 Bits of Useable Data Storage
- Non-Volatile, Solid-State Memory
- True Binary Organization — 512 Bit Page and 2048 Pages
- Serial-Parallel-Serial Architecture
- Redundant Loops with On-Chip Loop Map and Index
- Complete Set of Interface Circuits for Ease of Use
- Controller allows 128K Bytes to 1 Mega Byte Systems
- Easy Paralleling or Multiplexing of IM's Bubble Memories
- Transparent Burst Error Correction
- Single Chip 20-Pin Dual In-Line Leadless Package and Socket
- Small Physical Volume
- Low Power per Bit
- Maximum Data Rate Range 100kHz to 200kHz

Description

The Intel Magnetics 7110 is a very high density 1 Mega Bit non-volatile, solid-state memory utilizing the magnetic bubble technology. The usable data storage capacity is 1,048,576 bits. The defect tolerant design incorporates redundant storage loops. The gross capacity of Intel Magnetics bubble memory is 1,310,720 bits.

The 7110 has a true binary organization to simplify system design, interfacing, and system software. The device is organized as 256 data storage loops each having 4096 storage bits. When used with Intel Magnetics complete family of support electronics the resultant minimum system is configured as 128K Bytes of usable data storage. Also the support circuits provide automatic error correction and transparent handling of redundant loops.

The 7110 has a serial-parallel-serial architecture. It has separate read and write tracks. Logically, the data is organized as a 512 bit page with a total of 2048 pages. The redundant loop information is stored on-chip in the bootstrap loop along with an index address code. When power is disconnected, the 7110 retains the data stored and the bubble memory



Block Diagram of Single Bubble Memory System — 128K Bytes

7110, 7112

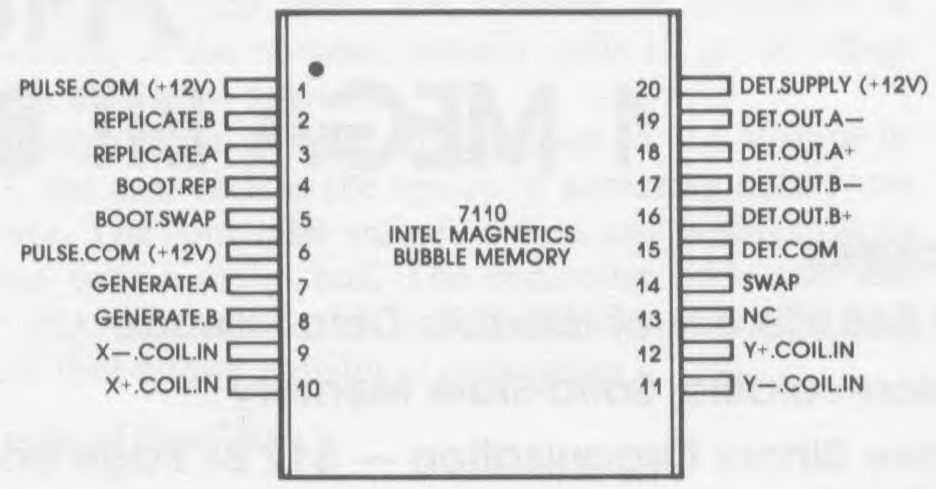
Description (Continued)

system is automatically restarted when power is restored via the support electronics.

The 7110 is packaged in a dual in-line leadless package complete with permanent magnets and coils for the in-plane rotating field. In addition, the 7110 has a magnetic shield surrounding the bubble memory chip to protect the data from externally induced magnetic fields.

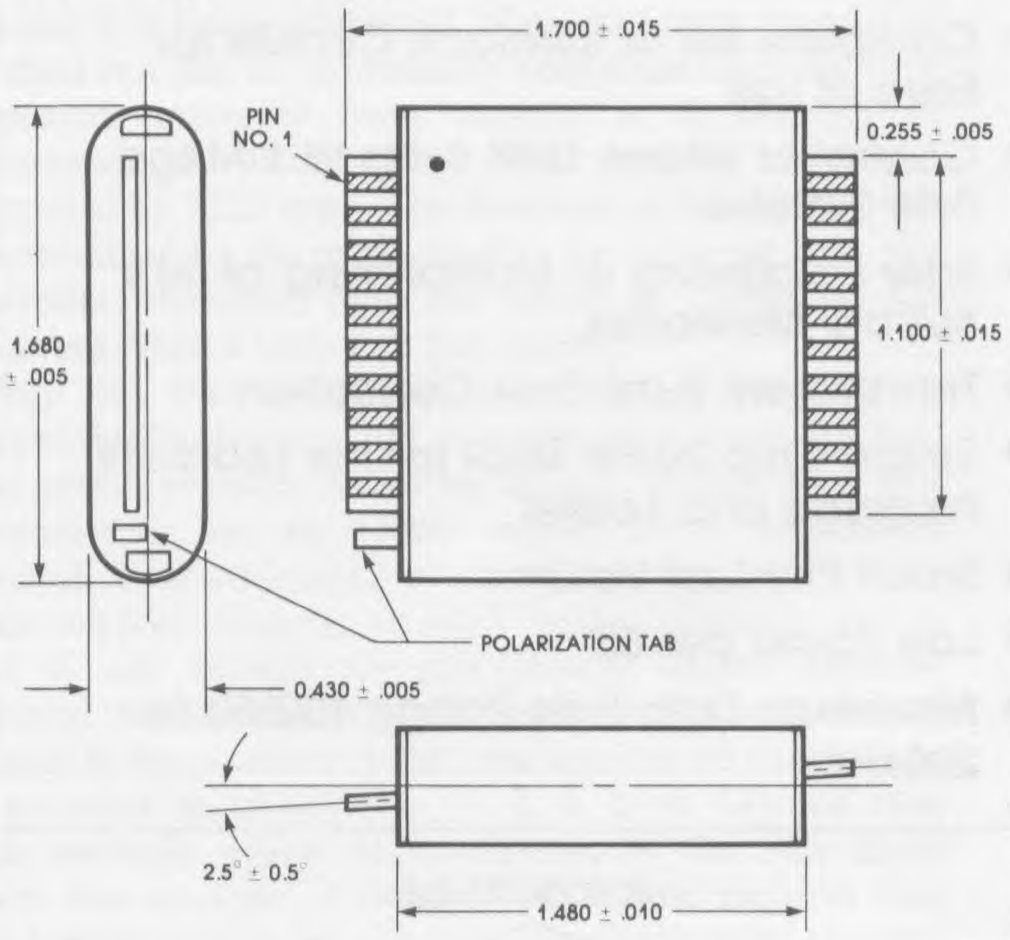
The 7110 operating data rate is 100kHz and the 7112 operates at 200kHz. Both bubble memories can be operated asynchronously and have start/stop capability.

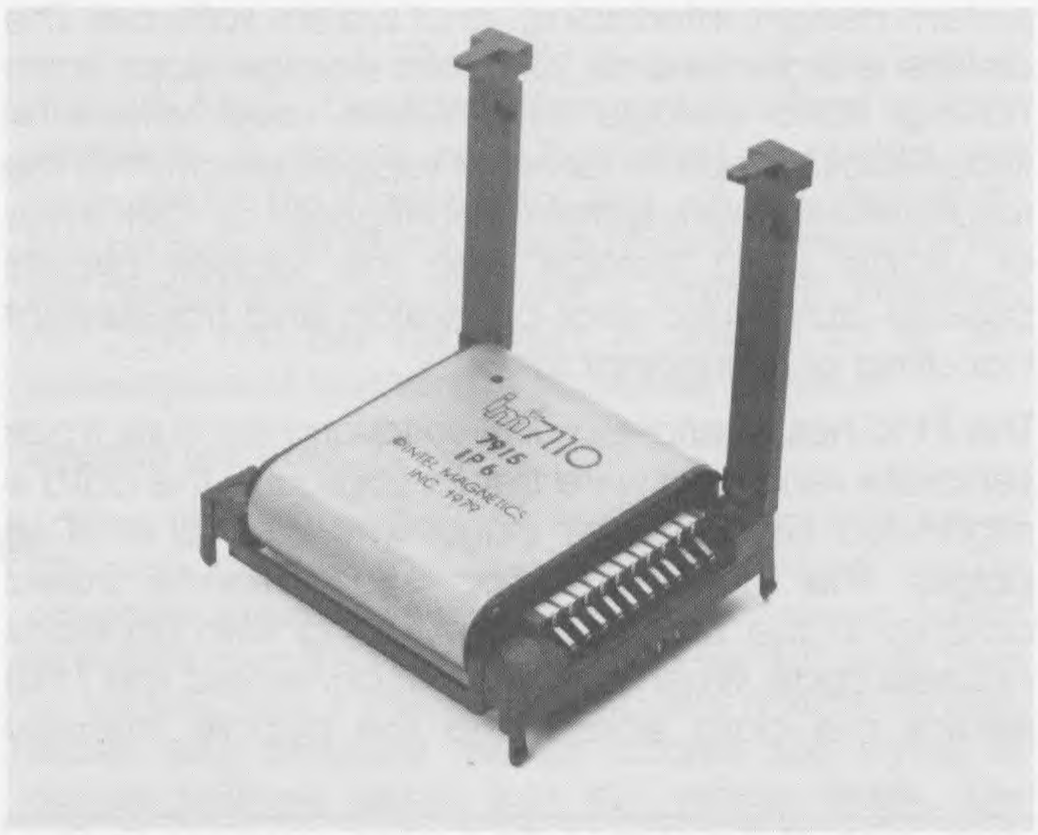
Pin Configuration



NOTE: PINS 1 AND 6 ARE NOT INTERNALLY CONNECTED AND PIN 13 SHOULD NOT BE USED AS A TIE POINT.

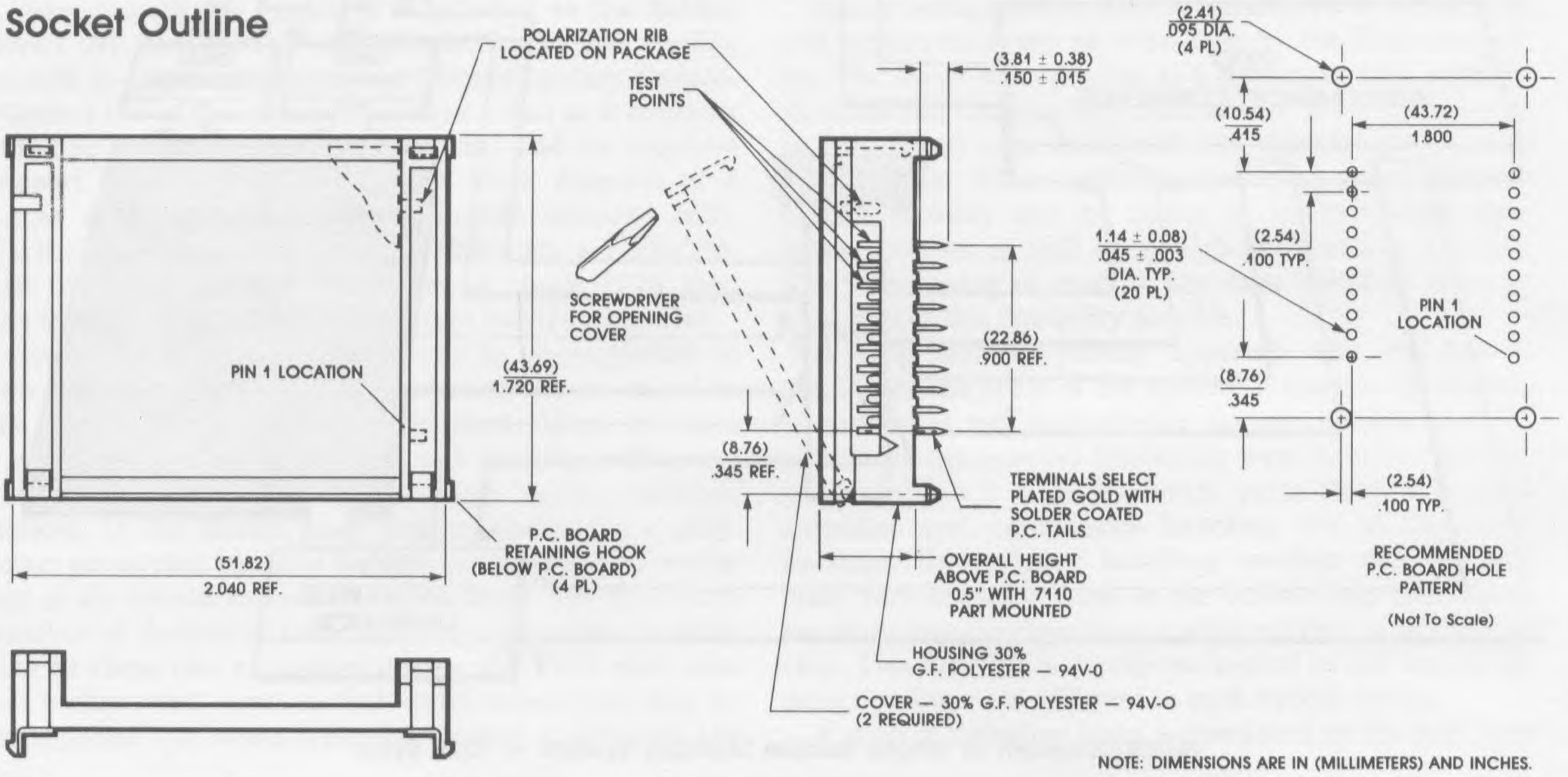
Package Outline





7110 Package Seated in Socket with Arms Up

Socket Outline



NOTE: DIMENSIONS ARE IN (MILLIMETERS) AND INCHES.

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7110, 7112

Bubble Memory Performance Options

	7110	7112
Max. Data Rate (kHz)	100	200
Nom. Data Rate (kHz)	68	136
Rotating Field Rate (kHz)	50	100
Avg. Access Time (ms)	40	20
Coil Voltage (V)	+12	+12

Pin Description

BOOT.REP (Pin 4)

Two-level current pulse input for reading the boot loop.

BOOT.SWAP (Pin 5)

Single-level current pulse for writing data into the boot loop. This pin is normally used only in the manufacture of the MBM.

DET.COM (Pin 15)

Ground return for the detector bridge.

DET.OUT (Pins 16 through 19)

Differential pair (A+, A— and B+, B—) outputs which have signals of several millivolts peak amplitude for a '1' (bubble) or noise for a '0' (no bubble).

DET.SUPPLY (Pin 20)

+12 volt supply pin.

GEN.A and GEN.B (Pins 7, 8)

Two-level current pulses for writing data onto the input track.

PULSE.COM (Pins 1, 6)

Two unconnected +12 volt supply pins.

REP.A and REP.B (Pins 3 and 2)

Two-level current pulses for replicating data from storage loops to output track.

SWAP (Pin 14)

Single-level current pulse for swapping data from input track to storage loops.

X—.COIL.IN, X+.COIL.IN (Pins 9, 10)

Terminals for the X or inner coil.

Y—.COIL.IN, Y+.COIL.IN (Pins 11, 12)

Terminals for the Y or outer coil.

D.C. and Operating Characteristics T_A = 0°C to 50°C unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Nom.	Max.		
R_1	Resistance: PULSE.COM to REP.A or REP.B	15	20	25	ohms	
R_2	Resistance: PULSE.COM to BOOT.REP	7	10	13	ohms	
R_3	Resistance: PULSE.COM to BOOT.SWAP	15	20	25	ohms	
R_4	Resistance: PULSE.COM to GEN.A or GEN.B	35	45	55	ohms	
R_5	Resistance: PULSE.COM to SWAP	40	55	70	ohms	
R_6	Resistance: DET.COM to DET.OUT.A+ or DET.OUT.B+	440	640	840	ohms	
R_7	Resistance: DET.COM to DET.OUT.A— or DET.OUT.B—	470	670	870	ohms	
R8	Resistance: DET.COM to DET.SUPPLY	360	510	660	ohms	
R_X	X Coil Resistance		5.2		ohms	
R_Y	Y Coil Resistance		2.7		ohms	
L_X	X Coil Inductance		100		μH	
L_Y	Y Coil Inductance		86		μH	

7110, 7112

Drive Requirements T_A = 0°C to 50°C unless otherwise specified.

Symbol	Parameter	7110			7112			Units
		Min.	Nom.[1]	Max.	Min.	Nom.[1]	Max.	
f_R	Field Rotation Frequency	49.995	50.000	50.005	99.99	100.00	100.01	kHz
ϕ_L	Phase Lag from Y.COIL to X.COIL	85	90	95	85	90	95	Degrees
I_{PX+}	X.COIL Positive Peak Current		550			1100		mA
I_{PX-}	X.COIL Negative Peak Current		550			1100		mA
I_{PY+}	Y.COIL Positive Peak Current		690			1380		mA
I_{PY-}	Y.COIL Negative Peak Current		690			1380		mA
P_T	Total Coil Power		1.3	TBD		TBD	TBD	W

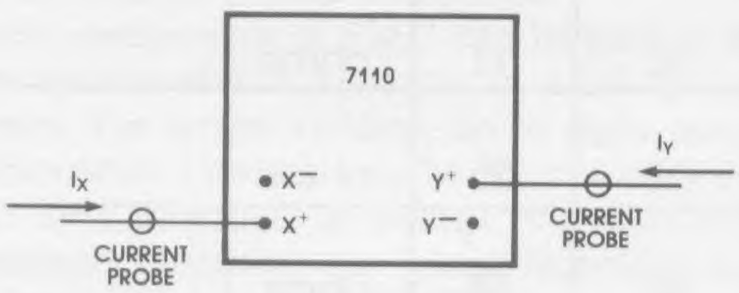
Note: 1. Nominal values are at T_A = 25°C.

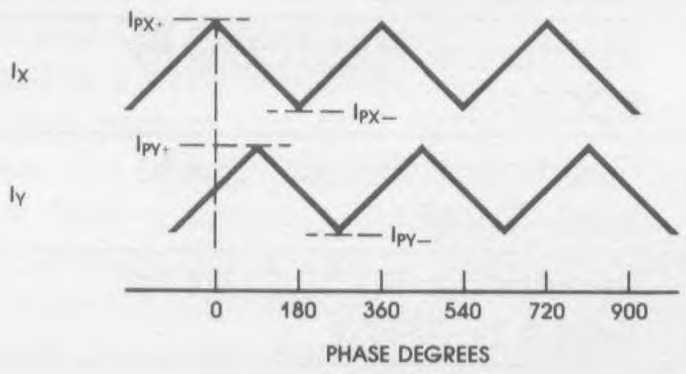
Control Pulse Requirements Nominal values at T_A = 25°C. See Notes 1 and 2.

Pulse	Amplitude (mA)	Phase of Leading Edge (Degrees)	Width (Degrees)
GEN.A, GEN.B Cut	130	270 (Odd), 90 (Even)	4.5
GEN.A, GEN.B Transfer	40	270 (Odd), 90 (Even)	54
REP.A, REP.B Cut	180	270	4.5
REP.A, REP.B Transfer	140	270	90
SWAP	140	180	450
BOOT.REP Cut	TBD	TBD	TBD
BOOT.REP Transfer	TBD	TBD	TBD
BOOT.SWAP	TBD	TBD	TBD

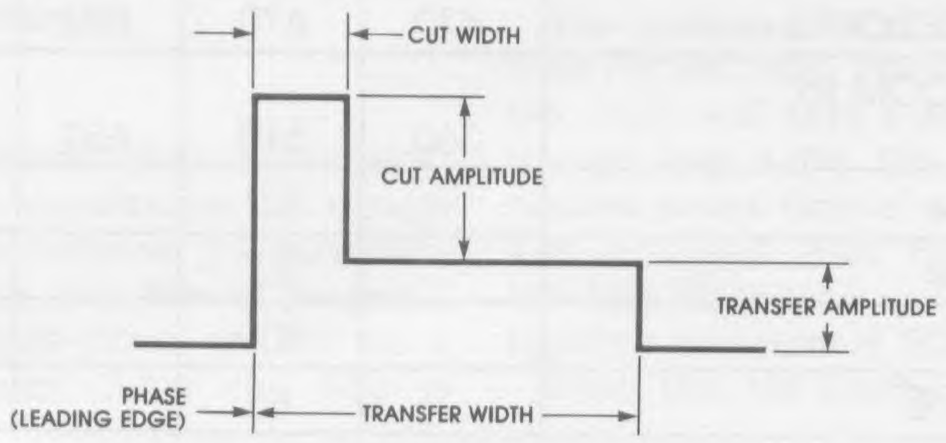
Notes:

1. Pulse timing is given in terms of the phase relations as shown below. For example, a 7110 operating at f_R = 50.000 kHz would have a REP.A transfer width of 90° which is 5μs.





2. Two level pulses are described as shown below.



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7110/7112

Preliminary

Absolute Maximum Ratings*

Ambient Operating Temperature ..... 0-50°C
Relative Humidity 95%
Non-Volatile Storage Temperature ..... TBD
Voltage Applied to DET.SUPPLY or PULSE.COM 14V
Continuous Current between PULSE.COM and Inputs 10mA
Continuous Current between DET.COM and Detector Outputs 10mA
Coil Current (7110) .... 1A Peak (Triangular), 0.5A D.C.
Coil Current (7112) ..... TBD

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

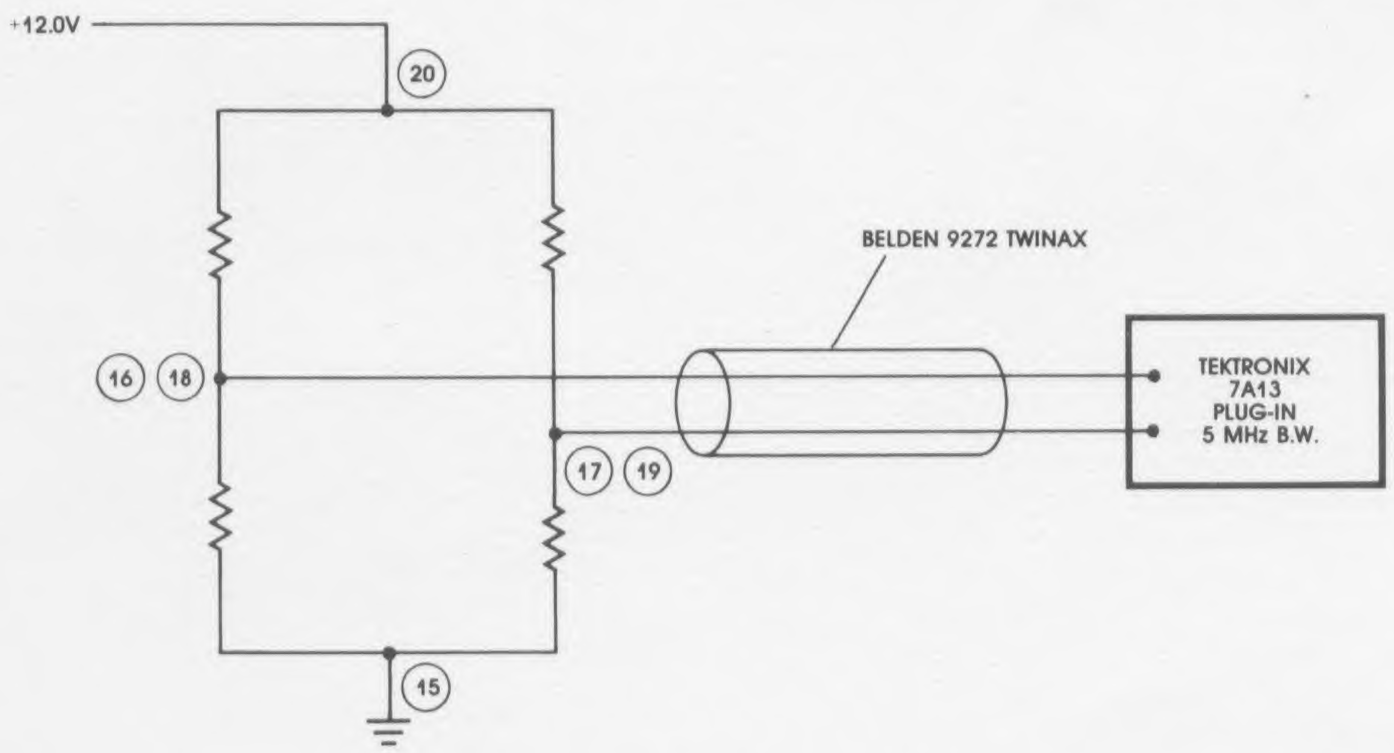
Environmental Specifications

	Min.	Nominal	Max.	Units
Weight (Without Socket)		74	80	Grams
External Magnetic Field		40	TBD	Oersteds
Non-Operating Handling Shock			200	G
Non-Operating Vibration (2 kHz)			20	G
Operating Vibration Up to 500KHz			TBD	G

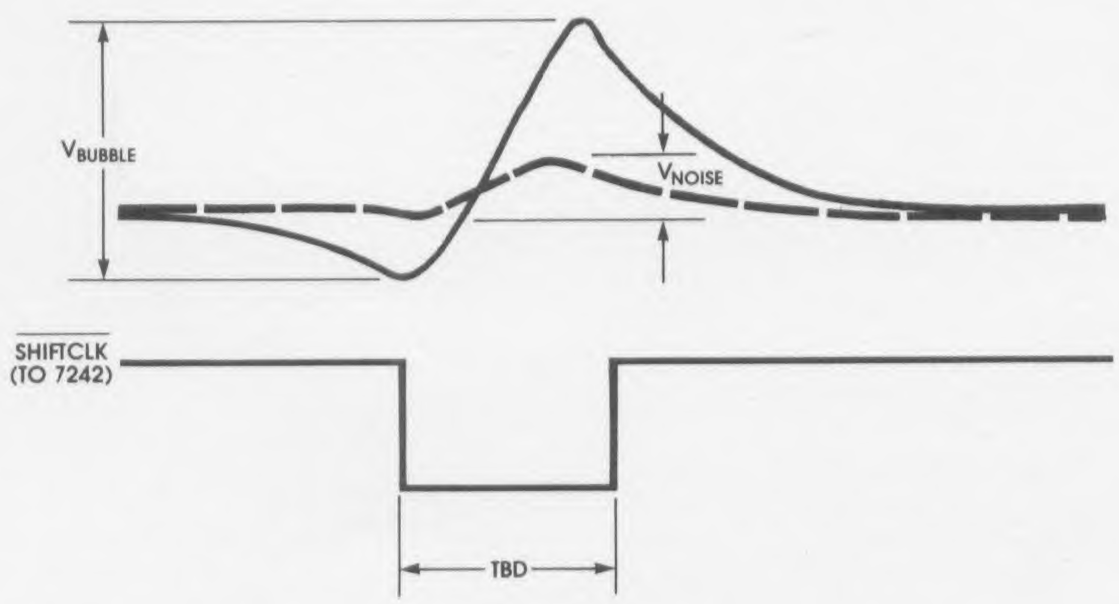
Output Characteristics

T_A = 25° C unless otherwise specified.

	Min.	Nom.	Max.	Units	Test Conditions
V_{BUBBLE}	TBD	8.0		mV	See Figures below.
V_{NOISE}		1.5	TBD	mV	



Test Set-Up for Output Voltage Measurement



Output Waveforms

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advance information

7220
BUBBLE MEMORY CONTROLLER

Features

- **Ideal for IM's Bubble Memories**
- **Standard 8080/8085/Multibus™ Interface**
- **Multiple Bubble Module Interface Capability**
- **Self-Contained Timing Generation**
- **DMA Handshake Capability**
- **Single or Multiple Page Block Transfers**
- **HMOS Technology**
- **Standard 40-Pin Dual In-Line Package**

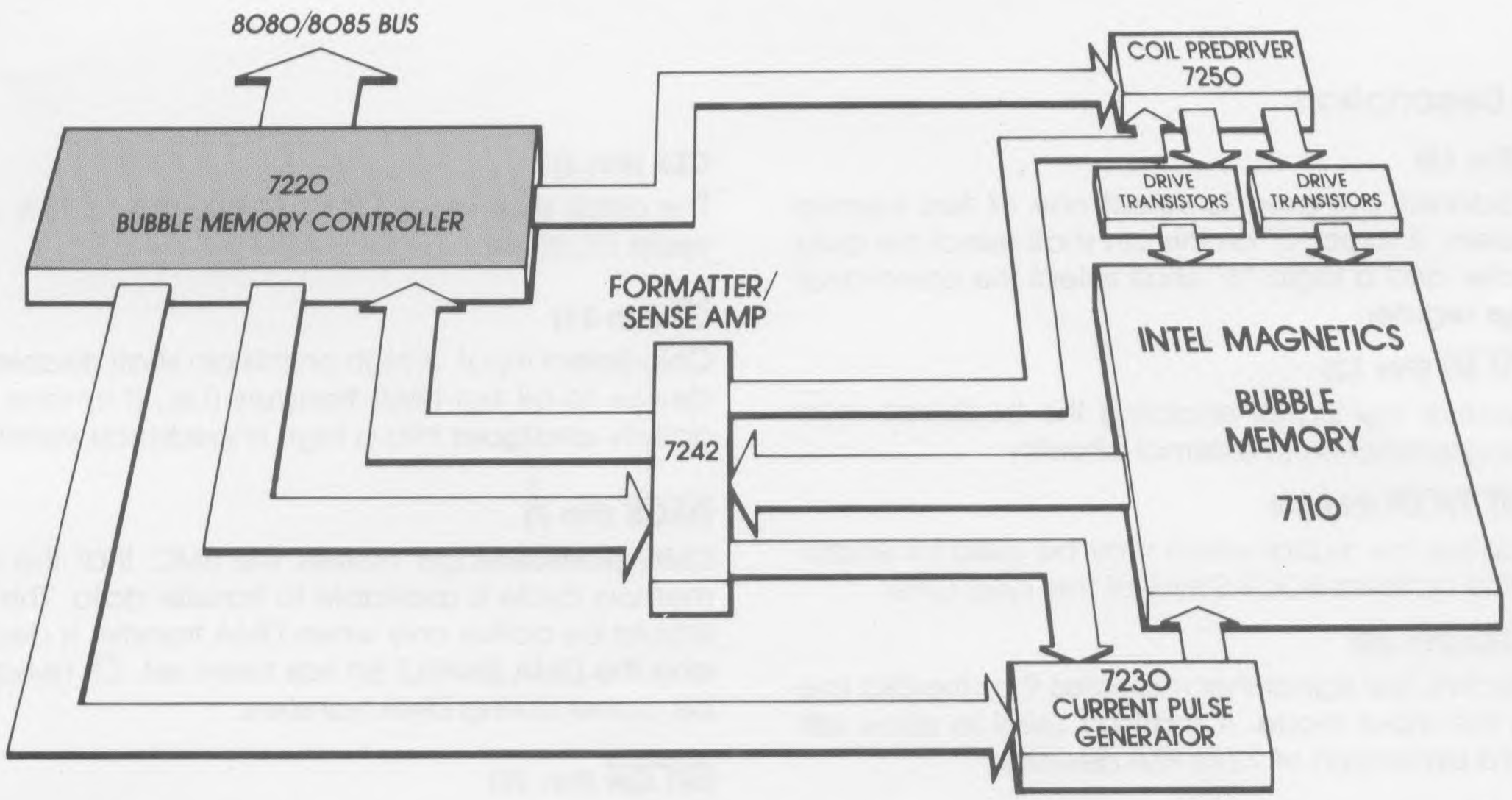
Description

The Intel 7220 is a complete Bubble Memory Controller (BMC) designed to interface with Intel Magnetics Bubble Memories. The interface to the outside world is through the standard 8080/8085/ Multibus™.

The 7220 is capable of multiple bubble memory interface. It has self-contained timing generation and DMA handshake capability. Single and/or multiple page block transfers are also possible.

The 7220 is capable of interfacing with up to eight 7242 Dual Formatter/Sense Amplifier (FSA) devices. Serial data from the bubble memory via the FSA is reformatted into a nine bit parallel bus (ninth bit can be used for parity) at the host CPU interface.

The 7220 utilizes Intel's high performance HMOS technology. The device is packaged as a standard 40-pin dual in-line package. All inputs and outputs are directly TTL compatible and the device uses a single +5 volt supply.



Block Diagram of Single Bubble Memory System — 128K Bytes

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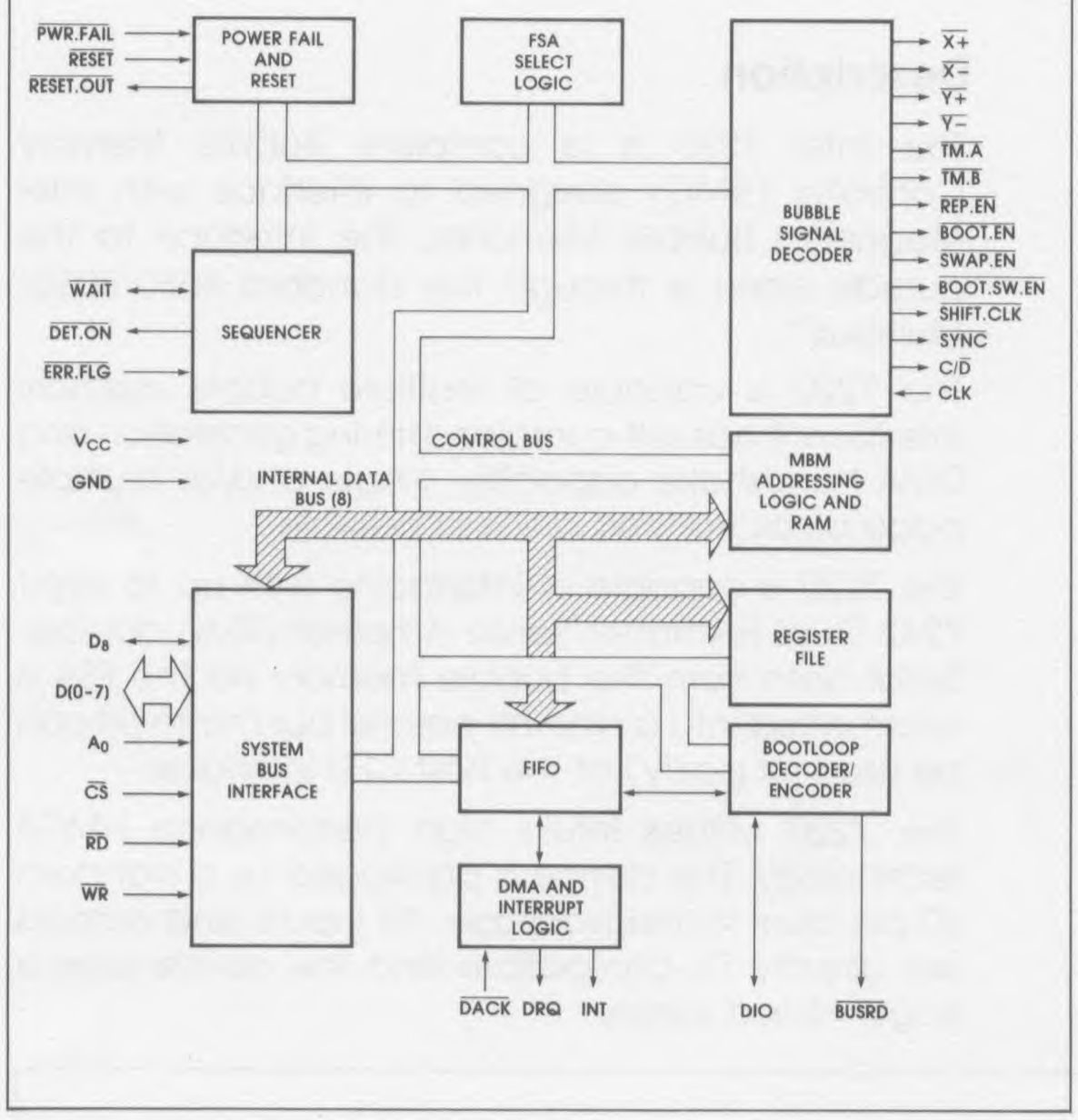
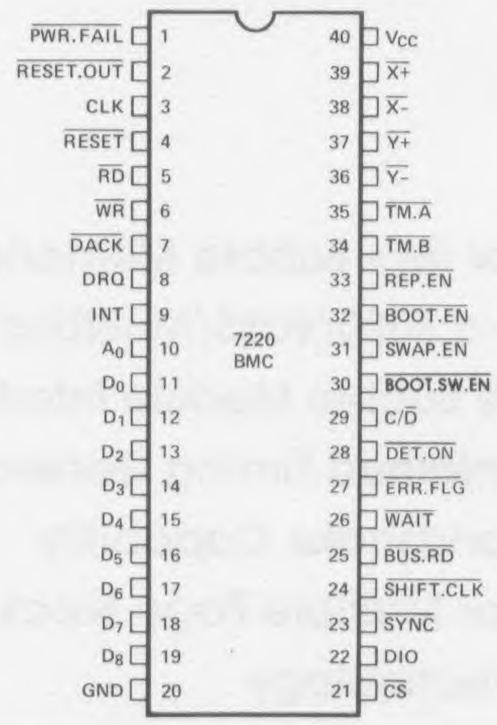
7220

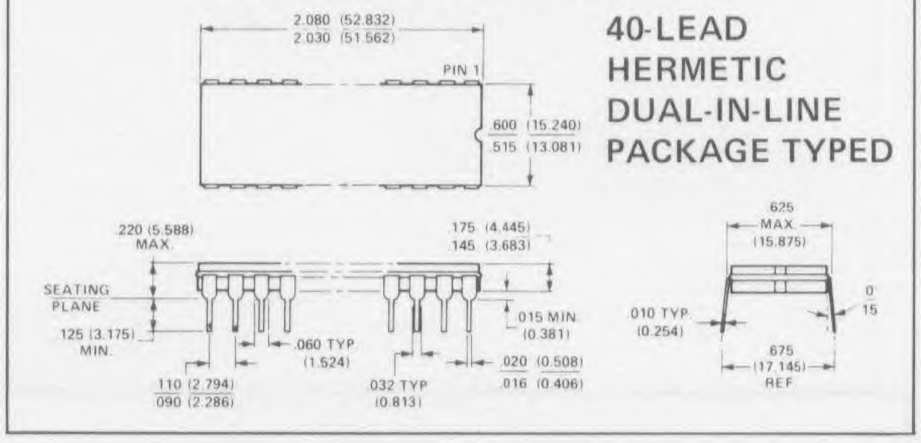
Logic Diagram



Pin Configuration



Packaging Information



Pin Description

A_0 (Pin 10)

An address pin used to select one of two internal registers. A logic "0" on this pin shall select the data register and a logic "1" shall select the command/ status register.

$\overline{\text{BOOT.EN}}$ (Pin 32)

An active low signal enabling the bootstrap loop replicate function in external circuitry.

$\overline{\text{BOOT.SW.EN}}$ (Pin 30)

An active low signal which may be used for enabling the optional BOOT.SWAP of the 7230 CPG.

$\overline{\text{BUS.RD}}$ (Pin 25)

An active low signal that indicates that the DIO line is in the input mode. It shall be used to allow off-board expansion of 7242 FSA devices.

C/$\overline{\text{D}}$ (Pin 29)

A high on this line shall indicate that the BMC is beginning command sequence.

CLK (Pin 3)

The clock shall be a 3.2 to 5 MHz, 50% ±10% duty cycle TTL clock.

$\overline{\text{CS}}$ (Pin 21)

Chip Select Input. A high on this pin shall disable the device to all but DMA transfers (i.e., it ignores bus activity and goes into a high impedance state).

$\overline{\text{DACK}}$ (Pin 7)

DMA acknowledge notifies the BMC that the next memory cycle is available to transfer data. This line should be active only when DMA transfer is desired and the DMA ENABLE bit has been set. $\overline{\text{CS}}$ need not be active during DMA transfers.

$\overline{\text{DET.ON}}$ (Pin 28)

An active low signal indicating that the magnetic bubble is detecting. It is useful for power saving in the MBM.

Pin Description (Continued)

DIO (Pin 22)
A bidirectional, active high data line that shall be used for serial communications with 7242 FSA devices.

DRQ (Pin 8)
A logic high shall indicate that a transfer of data between BMC and host memory is being requested.

D_0-D_8 (Pins 11 through 19)
A nine bit bidirectional port which can be read or written by utilizing the RD and WR strobes. D_0 shall be the LSB. D_8 shall be a parity signal. When a byte is transferred to the BMC (over D_0-D_7), odd parity shall be generated by the BMC and compared to D_8. When a byte is transferred from the BMC to the host, odd parity over D_0-D_7 shall be generated and transferred as D_8. Errors in parity shall create an interrupt when enabled by the host CPU.

$\overline{\text{ERR.FLG}}$ (Pin 27)
An active low input generated externally by 7242 FSA indicating that an error condition exists.

INT (Pin 9)
A logic one shall indicate that the BMC has a new status and requires servicing when enabled by the host CPU.

$\overline{\text{PWR.FAIL}}$ (Pin 1)
A logic zero shall indicate that power has failed. It shall force the BMC to begin a controlled stop sequence and hold it in an idle state as RESET does.

$\overline{\text{RD}}$ (Pin 5)
Enables BMC to output data to the data bus.

$\overline{\text{REP.EN}}$ (Pin 33)
An active low signal used to enable the replicate function in external circuitry.

$\overline{\text{RESET}}$ (Pin 4)
A logic zero on this pin shall force the BMC to an idle state and force all bubble memory interface signals to the logic one state (inactive).

$\overline{\text{RESET.OUT}}$ (Pin 2)
An active low signal that disables external logic. It shall be initiated by a $\overline{\text{PWR.FAIL}}$ or $\overline{\text{RESET}}$ signal, but shall not become active until the stopping point in a field rotation is reached (if the BMC is causing the bubble memory drive field to be rotated).

$\overline{\text{SHIFT.CLK}}$ (Pin 24)
A controller generated clock that initiates data transfer between selected FSA's and their corresponding bubble memory devices. The timing on $\overline{\text{SHIFT.CLK}}$ shall vary depending upon whether data is being read or written to the bubble memory.

$\overline{\text{SWAP.EN}}$ (Pin 31)
An active low signal used to create the swap function in external circuits.

$\overline{\text{SYNC}}$ (Pin 23)
An active low output utilized to create time division multiplexing slots in a 7242 FSA chain. It shall also indicate the beginning of a data or command transfer between BMC and 7242 FSA.

$\overline{\text{TM.A}}$ (Pin 35)
An active low timing signal generated by the decoder logic for determining CUT pulse width.

$\overline{\text{TM.B}}$ (Pin 34)
An active low timing signal generated by the decoder logic for determining TRANSFER pulse width.

$\overline{\text{WAIT}}$ (Pin 26)
A bidirectional pin that shall be tied to the WAIT pin on other BMC's when operated in parallel. It shall indicate that an error has been detected and that the BMC's should halt until the type of error has been determined. An active low signal.

$\overline{\text{WR}}$ (Pin 6)
Enables BMC to receive data from the data bus.

$\overline{\text{X+,X-,Y+,Y-}}$ (Pins 39, 38, 37 and 36)
Four active low timing signals generated by the decoding logic and used to create coil drive currents in the bubble memory device.

Functional Description

Each block of the 7220 BMC is briefly described as follows:

System Bus Interface — The System Bus Interface (SBI) logic contains the timing and control logic required to interface the BMC to a non-multiplexed bus. The logic also contains the circuitry to check and generate parity (odd) on transfers across the bus. The interface has input data, output data, and status data latches. The SBI communicates with other BMC sections including parameter registers via the 8-bit internal data bus.

Functional Description (Continued)

FIFO — The FIFO is a 40×8 bit FIFO RAM for data storage. The FIFO RAM is dual port so that data may be read (written) at one port while simultaneously being written (read) at the other. It will be the responsibility of the host to make sure there is data/room available in the FIFO for transfers to/from the FSA's. If the host fails to keep up a timing error will result. The FIFO block also contains input and output data latches, providing double data buffering, to improve the R/W cycle times seen at the SBI (minimum 600 nsec cycle time). The FIFO may be used as a general purpose FIFO when a command is not being executed by the BMC Sequencer. In this mode, the FIFO ready status bit will become a FIFO absolutely empty indicator.

DMA and Interrupt Logic — The BMC DRQ pin has two functions:

(1) If the DMA enable bit in the enable register is set, the DRQ pin, in conjunction with the $\overline{\text{DACK}}$ pin, provides a standard DMA transfer capability, i.e., it has the ability to handshake with an 8257 or 9517 DMA controller chip.

(2) If the DMA enable bit is reset, the DRQ pin acts as a "ready for data transfer interrupt" pin. It becomes active when 20 bytes may be read from/written into the BMC, it is reset when this condition no longer exists.

This interrupt mode offers an alternative to polling the status word in medium performance systems when DMA is not used.

Bootloop Decoder/Encoder — This block of circuitry does parallel to serial and serial to parallel conversion of data to generate the bidirectional DIO pin, which is the data bus line to FSA's in the Bubble system. It also generates the $\overline{\text{BUSRD}}$ pin which identifies the direction of DIO data transfer if external buffering is required for the DIO line. This block also contains hardware to generate and decode the Bubble Bootstrap loop code during Read and Write Bootloop operations.

Sequencer — The BMC contains a microsequencer for control. The sequencer, by decoding the contents of the ROM, interprets commands, sets and resets flags and status bits, and initiates and terminates actions in other parts of the BMC.

MBM Addressing Logic and RAM — The address control logic contains the address of the next available page of data for up to 8 FSA's. The address maintained is the address available for a READ operation. The address for a WRITE operation is calculated by adding a constant to the READ address. The address control logic also contains circuitry to enable multiple page transfers of up to 2048 pages in length.

Register File — The register file contains 7 eight-bit registers that are accessible by the host CPU. Refer to the Register Section for details.

Bubble Signal Decoder — The bubble signal decoder logic contains logic for creating all timing signals for internal use as well as bubble memory timing. The logic consists of counters and decoder circuits. The counter logic consists of three stages. The first stage is a divide-by-four counter that is enabled or disabled by the host CPU. This counter will be used in low frequency systems to provide higher resolution timing. The second stage is a modulo forty counter. The input to this stage can be either the input clock or the output of the modulo four counter. These two counters are used to provide high resolution timing for bubble functions.

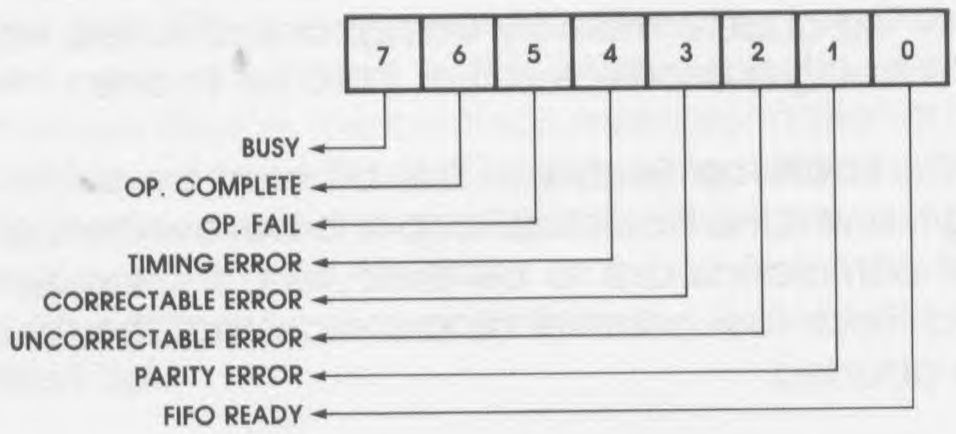
The third stage of the counter is a 12 bit counter whose input is the output of the second stage. It is used to count field rotations. It can be preset or cleared by the sequencer. The decoder provides the high speed timing pulses required by the bubble memory and for internal usage. Each signal can be set or reset on any edge of the forty increments of a field rotation (provided by the second stage counter). In addition, some outputs are capable of lasting for more than one field rotation (see Figure 1). Each signal is enabled or disabled by the sequencer. The outputs of each signal are latched or otherwise designed to be glitch-free.

FSA Select Logic — This logic determines which FSA's contain the addressed data. Information is obtained from the upper order bits of the block length register and address register (see Register Section). The output information is used by the Bootloop Decoder/Encoder to determine when valid data is available, or should be loaded, on the DIO line.

Powerfail and Reset — This circuit provides a means of resetting the BMC, and other system hardware via $\overline{\text{RESET.OUT}}$ pin, to a known or start state. $\overline{\text{PWR.FAIL}}$ is monitored by the sequencer on each cycle. When activated, a controller shutdown cycle is started immediately to assure bubble data integrity.

Registers

Directly Addressable Registers — There are two registers in the BMC that are directly read or written from the data bus. They are a status/command register and a data register. The status/command register is addressed by taking address line A_0 to a logic one and the data register by taking it to a logic zero. The status/command register is actually two separate registers. The status is read when this register is read and the command register can be written by writing into this register. The format of the bits in the status register is:



BUSY — This bit indicates that the controller sequencer is still in the process of executing its last command. When the controller is ready to receive a new command the bit is set low.

OP COMPLETE — This bit is set upon successful completion of a command. It is reset whenever the status register is interrogated by the host.

OP FAIL — A logic one in this bit indicates that the BMC was unable to successfully complete a command.

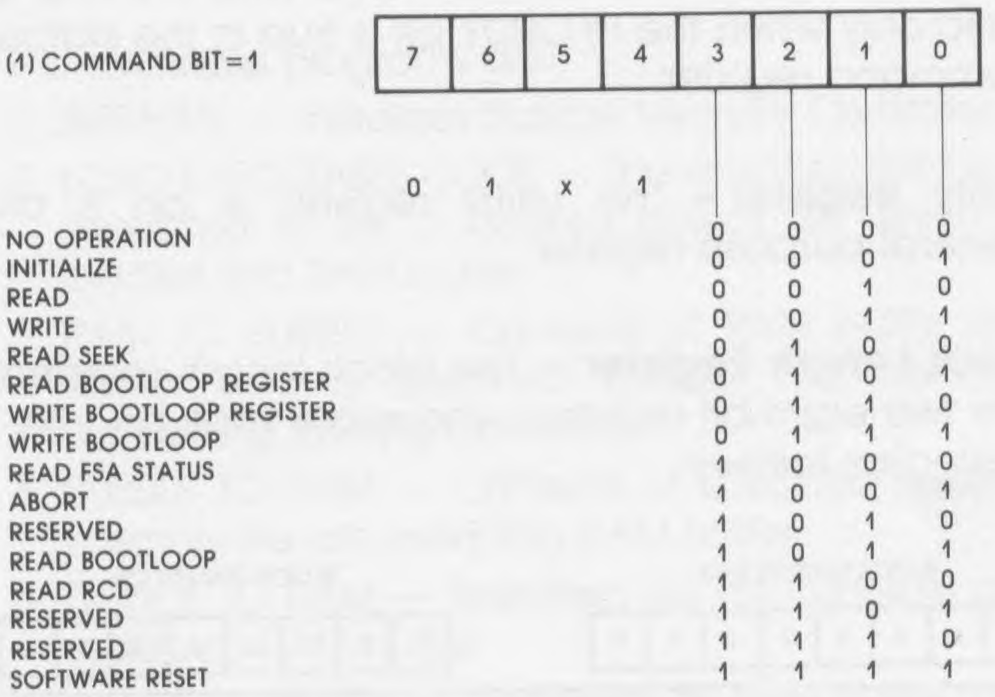
TIMING ERROR — This bit indicates that an FSA has reported a timing error, or the host has failed to keep up with the BMC and the BMC FIFO has overflowed or gone empty.

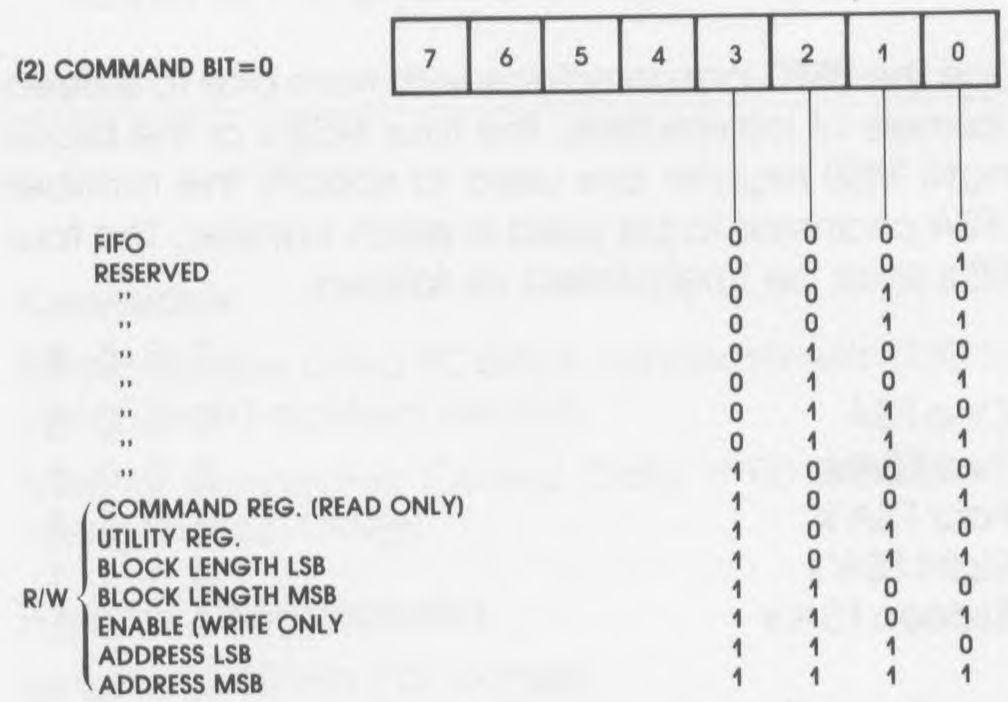
CORRECTABLE ERROR — Indicates that an FSA has reported a correctable error and shall be reset upon interrogation.

UNCORRECTABLE ERROR — Indicates that the last data block transferred contained an uncorrectable error. It shall be reset upon interrogation.

PARITY ERROR — Indicates a parity check failure and shall be reset upon interrogation.

FIFO READY — This bit indicates that the FIFO is available to be written or has data ready to be read when the busy bit is active. It indicates that the FIFO and FIFO input and output registers are all empty when busy is inactive. The Command Register serves a dual purpose. If bit 4 is a logical 1, bits 0–3 will be loaded as a BMC command. If bit 4 is a logical 0, then bits 0–3 will be loaded into the address latch. The four LSB's should be interpreted as follows:





Data Register — The source or destination of data read from or written to the data register is specified by first writing to the status/command register with bit 4=0 and bits 0–3 set corresponding to the desired register. The data then may be transferred by addressing the data register. For example, to read the ADDRESS LSB register of the BMC, the CPU must first write the bit pattern XXX01110 to the status/command register.

The CPU may then read the ADDRESS by addressing the data register (Pin A0=0) and performing a read operation. If the FIFO is selected as source or destination, then sequential FIFO locations shall be accessed with sequential reads or writes (only one status/command operation required). Otherwise, sequential registers are accessed with sequential

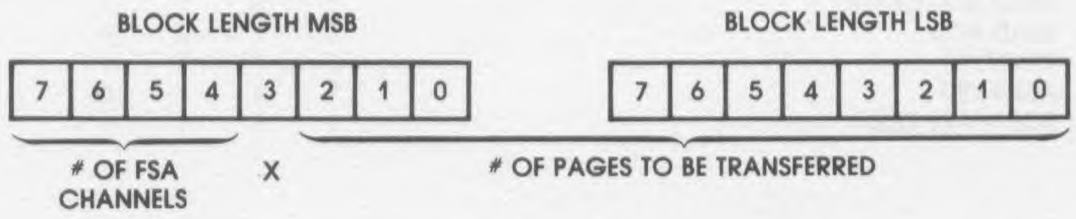
Registers (Continued)

reads or writes (e.g., COMMAND REG, BLOCK LENGTH LSB, etc.). Again, only one status/command operation is required.

FIFO Register — Data read or written into the FIFO is valid only when the FIFORDY bit is true in the status/command register.

Utility Register — The utility register is an 8 bit general purpose register.

Block Length Register — The block length registers are two eight-bit registers whose bits shall be interpreted as follows:

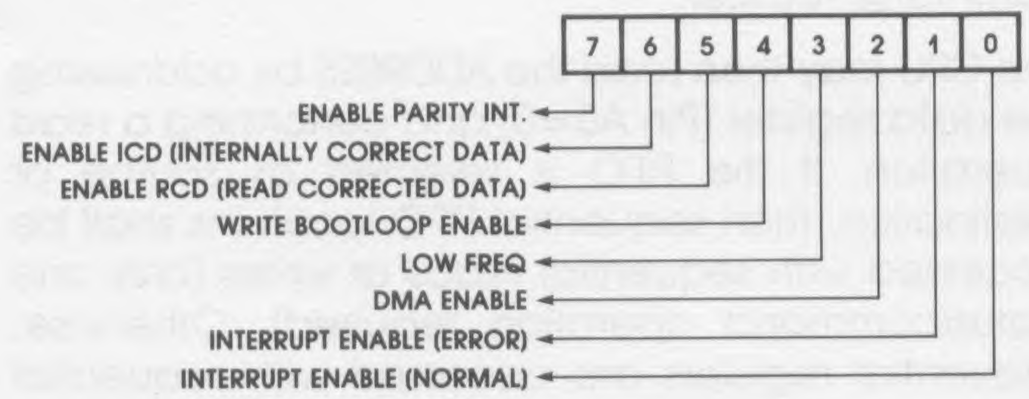


Since the BMC can interface with from one to sixteen channels of information, the four MSB's of the block length MSB register are used to specify the number of FSA channels to be used in each transfer. The four MSB's shall be interpreted as follows:

	7	6	5	4
One FSA	0	0	0	0
Two FSA's	0	0	0	1
Four FSA's	0	0	1	1
Eight FSA's	0	1	1	1
Sixteen FSA's	1	1	1	1

These four bits, in conjunction with the address bits, determine which memory modules are being accessed for a given transfer.

Enable Register — The enable register contains flags set by the host that will enable or disable various functions within the BMC or FSA. The bits in the register are interpreted as follows:



Interrupt Enable (Normal) — A logic one shall enable the BMC to interrupt the CPU upon completion of a task with the INT pin.

Interrupt Enable (Error) — A logic one shall permit the BMC to interrupt the CPU upon detection of an error condition, independent of its correctability, via the INT pin.

DMA Enable — A logic one shall cause the BMC to request data transfers via DRQ and $\overline{\text{DACK}}$ signals. A logic zero shall cause all transfers to occur via polling the status register or using DRQ as an interrupt pin. Refer to functional description for DMA and Interrupt Logic.

Low Freq — This bit shall be set to enable operation of the divide by four counter in the timing circuitry. Only the bubble memory timings are affected; host CPU timing is unaffected. For 7110 set to one.

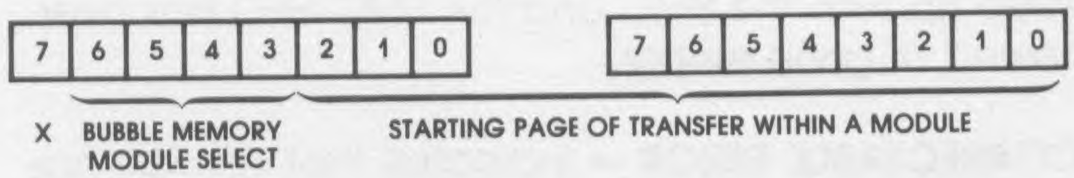
Write Bootloop Enable — This bit must be set to a logic one if the bootstrap loop is to be rewritten, or if test commands are to be executed. If it is a zero, and these four commands are received, they shall be aborted.

Enable RCD — Enables the BMC to attempt to correct the data as it is passed to the BMC. In the event of an uncorrectable error bad data may be passed to the host.

Enable ICD — Enables the BMC to attempt correction of data errors before transferring the data containing the error into host memory.

Enable Parity Interrupt — Enables the BMC to interrupt the host CPU upon detection of a parity error on the data bus.

Address Registers — The address registers consist of two eight bit registers whose bits are interpreted as follows:



The eleven LSB's designate the starting page address of the data transfer, regardless of the number of memory modules being accessed. The four MSB's, along with the four MSB's of the block length register determine which modules are to be accessed. Table 1 designates the FSA's that are to be used with various combinations of address and block length MSB's.

Table 1
FSA Channels Selected vs Address Bits

Block Length MSB	0000	0001	0011	0111	1111
Address MSB					
0 0 0 0	0	0, 1	0, 1, 2, 3	0 to 7	ALL
0 0 0 1	1	2, 3	4, 5, 6, 7	8 to 15	
0 0 1 0	2	4, 5	8, 9, 10, 11	—	
0 0 1 1	3	6, 7	12, 13, 14, 15	—	
0 1 0 0	4	8, 9	—	—	
0 1 0 1	5	10, 11	—	—	
0 1 1 0	6	12, 13	—	—	
0 1 1 1	7	14, 15	—	—	
1 0 0 0	8	—	—		
1 0 0 1	9	—	—		
1 0 1 0	10	—	—	—	
1 0 1 1	11	—	—	—	
1 1 0 0	12	—	—	—	
1 1 0 1	13	—	—	—	
1 1 1 0	14	—	—	—	
1 1 1 1	15	—	—	—	

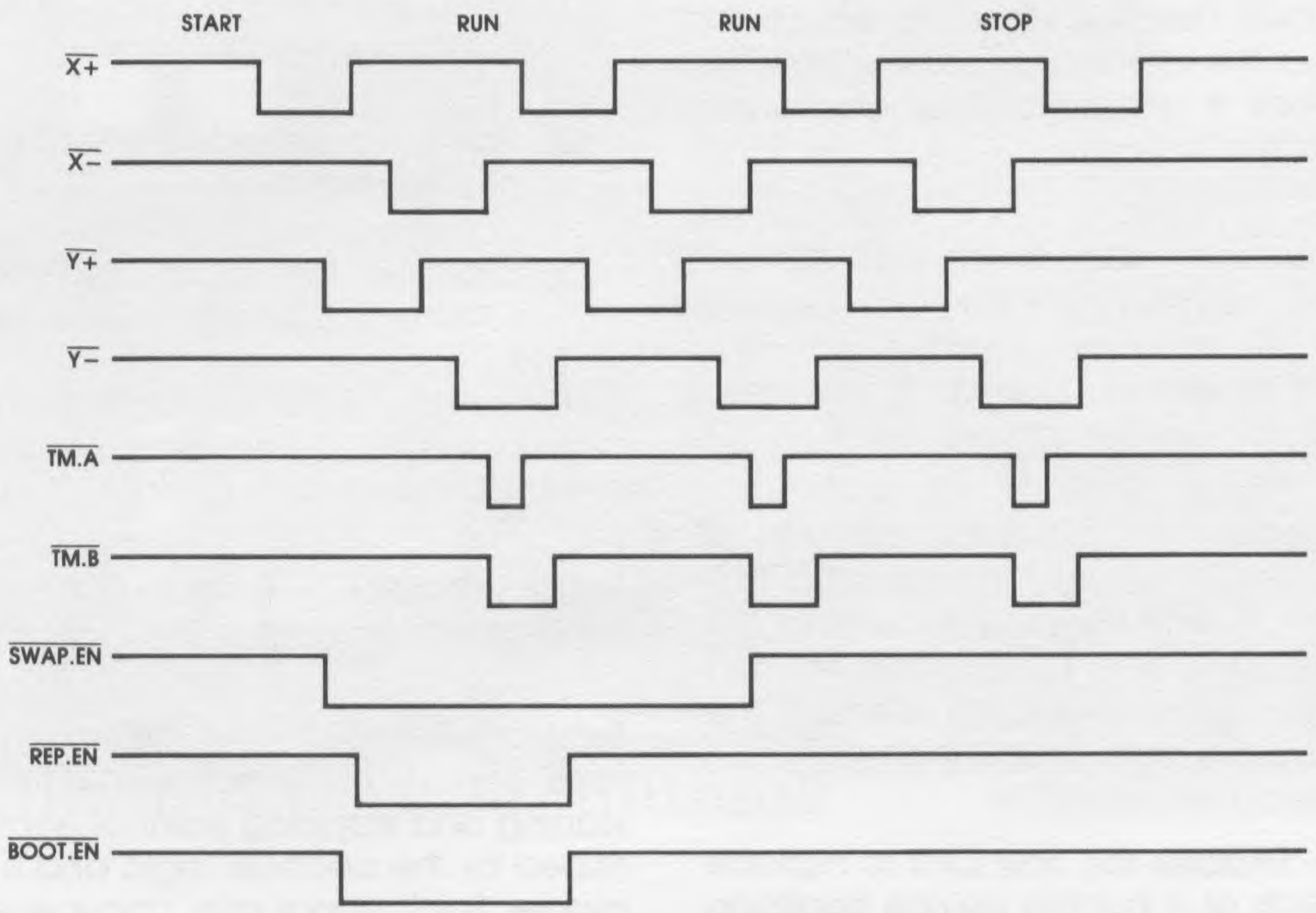


Figure 1. Typical Bubble Timing Signals

Commands

When a command is sent the BMC will be busy executing that command until 1) it is completed, 2) a fatal error occurs, or 3) an ABORT command is sent. The commands are briefly described as follows:

No-Operation — Causes the BMC to enter an idle state.

Initialize — Causes the BMC to read the contents of the bootstrap loop on each bubble device and store the contents in the associated FSA bootstrap loop register. The memory devices shall be stopped at a known address to be consistently defined as page address zero.

Read — Causes data to be transferred from bubble memory to BMC FIFO. Data is transferred from each bubble device selected per Table 1.

Write — Causes data to be transferred from BMC FIFO to bubble memory. Again, data is transferred to each bubble device per Table 1.

Seek — Causes the BMC to rotate the selected bubble device to the address specified and stop (no data transfers occur). The BMC stops the devices in such a manner that the selected address will be the first available block if a read to that address is specified.

Read Bootloop Register — Causes the BMC to read the contents of the selected FSA's bootloop register and store in FIFO. The data shall then be available to the host CPU. If more than one FSA is selected, bootloop register data will be interleaved.

Write Bootloop Register — Causes the contents of the BMC FIFO to be written into the selected FSA bootloop register. Twenty bytes are needed for each FSA selected since only 160 bits are required per FSA. Again, if more than one FSA is selected, the host must interleave the data properly.

Write Bootloop — Enables the host CPU to replace the existing contents of a bubble device bootloop with data stored in the BMC FIFO. Encoding is done in hardware so only 40 bytes of data are required. As a precaution, this command shall also require an enable bit be set in the enable register.

Read FSA Status — Causes the BMC to interrogate the status of all FSA's and store in the BMC FIFO. Note that the entire status of all FSA's can be read and stored in the first 16 bytes of the BMC FIFO with one command. The host CPU shall then have access to FSA status.

Software Reset — Resets all registers and the FIFO except initialization parameters.

Abort — Terminates present BMC activity.

Read Bootloop — Causes the BMC to read the selected bubble device bootstrap loop, decode, and store the results in the FIFO.

Read RCD — Commands Formatter to output corrected data which is in FSA's FIFO.

Interfaces

CPU Interface — The BMC can interface asynchronously to the host CPU. With a 5 MHz clock, it is capable of sustaining a 1.6 Mbyte/sec transfer rate, while data/room is available in the BMC FIFO.

Software Interface — The general procedure for communicating with the BMC is:

(1) Read the status/command register until BMC is not busy.

(2) Pass parameters to the BMC by addressing the proper register.

(3) Examine the status register to determine whether the operation was successful.

Commands, status, and parameters shall be passed via I/O commands. Data can be passed either I/O commands or via a DMA channel.

Serial Interface — Refer to 7242 FSA Specification for a description of the BMC/FSA interface.

Bubble Interface — The BMC/bubble memory interface consists of 10 active low timing signals. The starting and stopping point of each signal is determined by the decoder logic and is mask programmable. Each signal may occur every field rotation or only once in a number of field rotations. The field rotation in which a timing pulse occurs is controlled by the sequence logic. Figure 1 illustrates typical timing signals.

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Preliminary

7230
CURRENT PULSE GENERATOR FOR BUBBLE MEMORIES

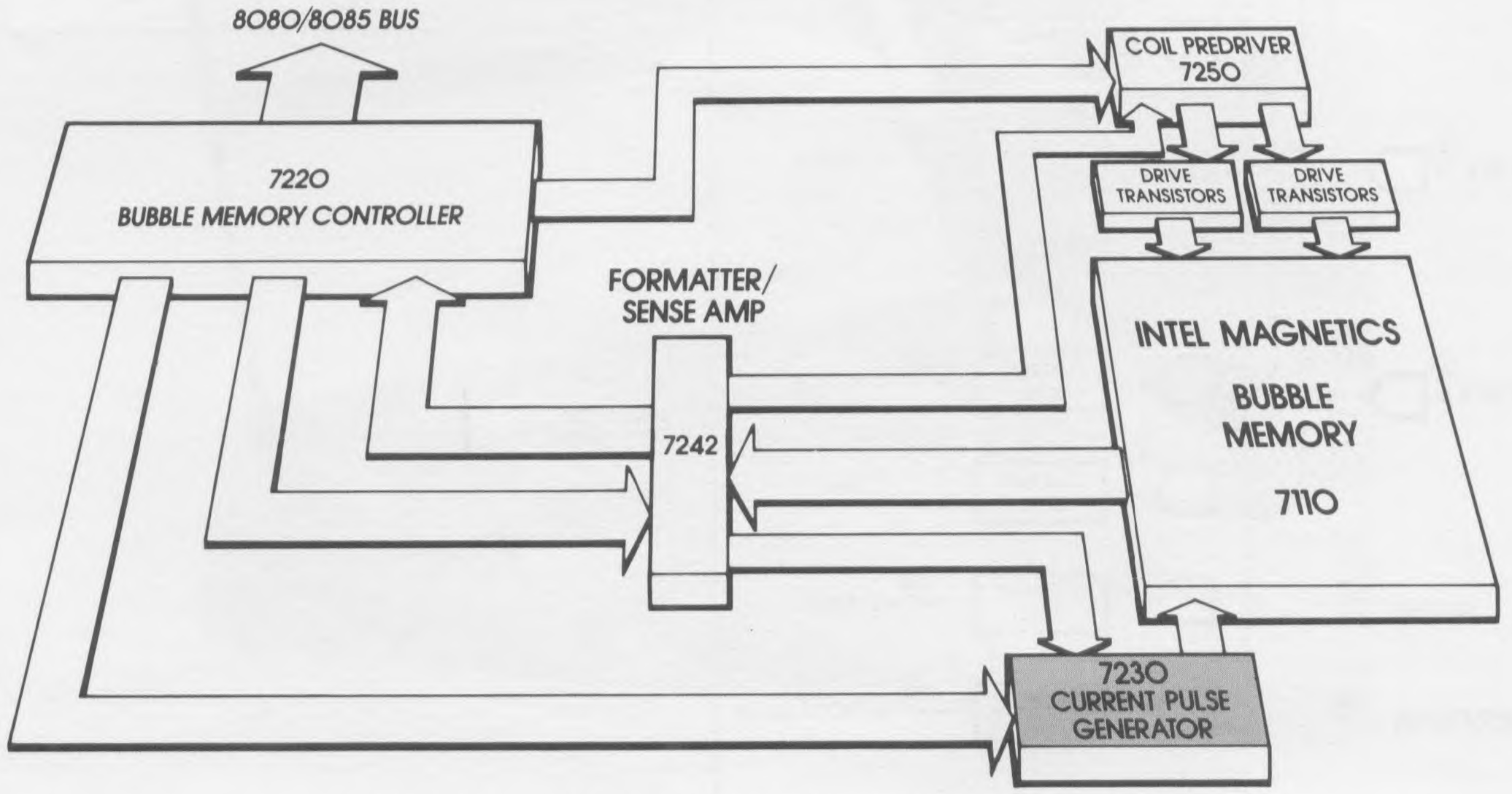
Features

- **Ideal for Use with IM's Bubble Memories**
- **TTL Compatible Inputs**
- **Provides all Pulses for IM's Bubble Memories**
  - **Replicate, Swap, Generate, and Boot Replicate**
- **Current Sink Outputs Designed to Directly Drive Bubble Memory**
- **Direct Interface to Bubble Memory Controller**
- **Power Down and Power Fail Signal**
- **Operates from +5 and +12 Volts Only**
- **Schottky Bipolar Technology**
- **Standard 22-Pin Dual In-Line Package**

Description

The Intel 7230 is a Current Pulse Generator (CPG) designed to drive Intel Magnetics Bubble Memories. The 7230 is a Schottky Bipolar, TTL input compatible device that converts digital timing signals to analog current pulses ideally suited for bubble memories. The CPG provides all pulses for Intel Magnetics Bubble Memories 7110 and 7112. These include Replicate, Swap, Generate, and Boot Replicate pulses. The high current sinking outputs directly drive the bubble memory. It also directly interfaces to the Intel Magnetics Bubble Memory Controller (BMC).

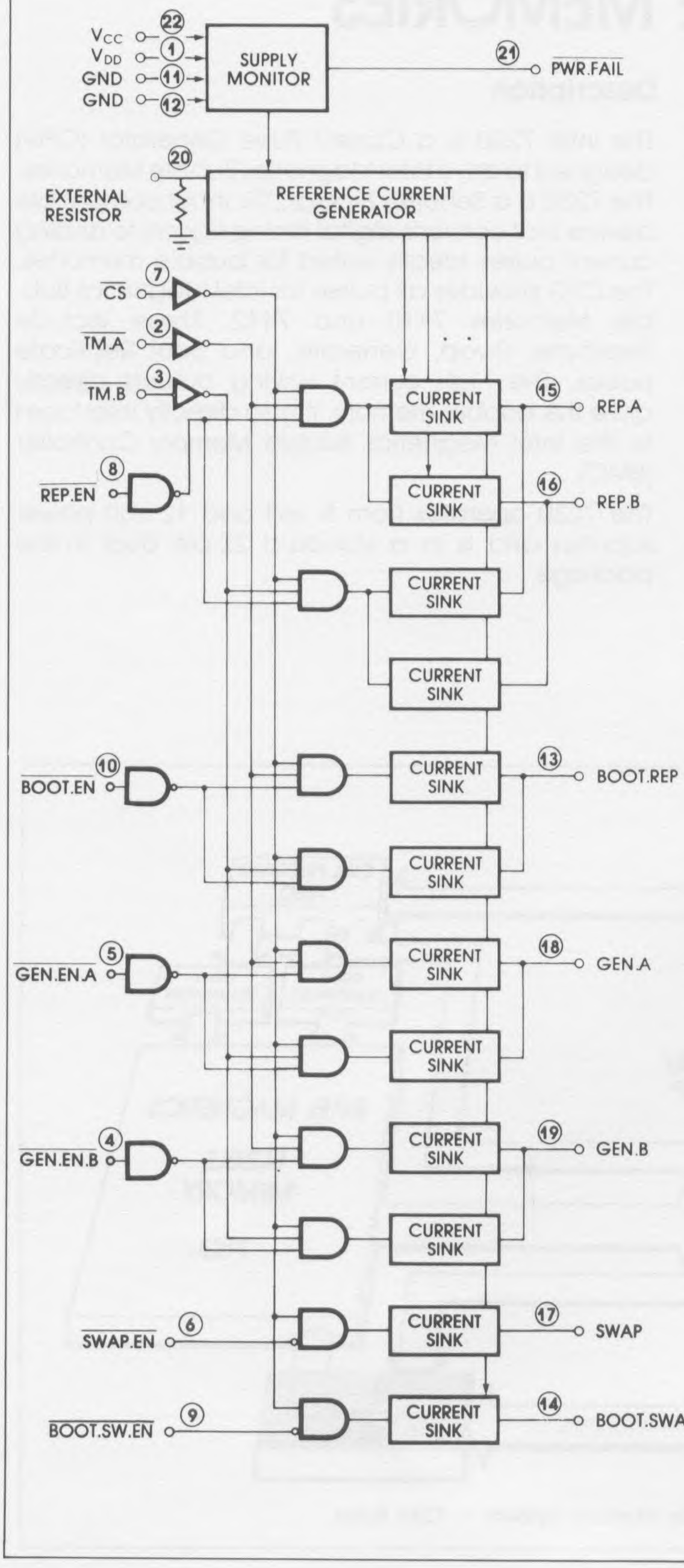
The 7230 operates from 5 volt and 12 volt power supplies and is in a standard 22-pin dual in-line package.



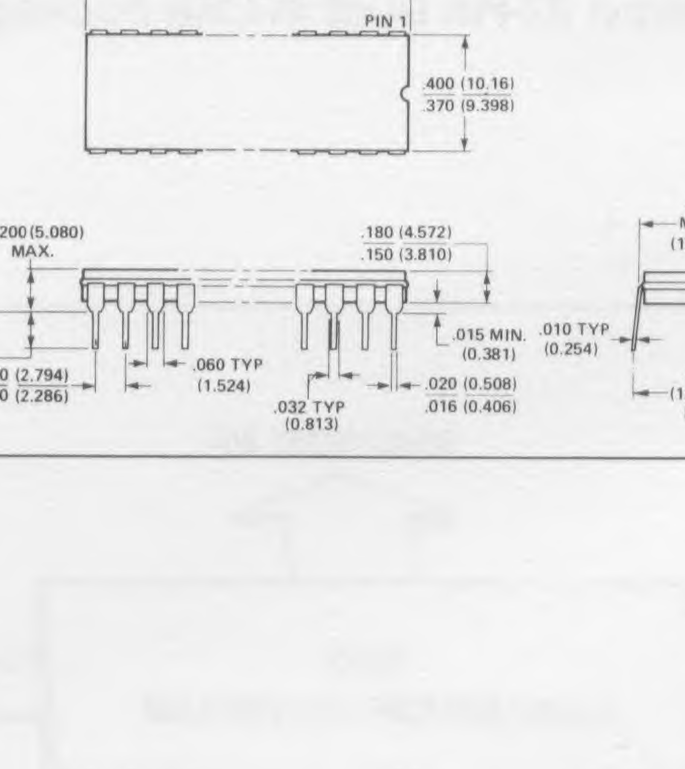
Block Diagram of Single Bubble Memory System — 128K Bytes

7230

Logic Diagram



Pin Configuration



Packaging Information
22-Lead Hermetic Dual-In-Line
Package Type D

Pin Description

$\overline{\text{BOOT.EN}}$ (Pin 10)
An active low input enabling the BOOT.REP output current pulse.

BOOT.REP (PIN 13)
An output providing the current pulse for bootstrap loop replication in the bubble memory.

BOOT.SWAP (Pin 14)
An optional output providing a current pulse which may be used for writing data into the bootstrap loop.

$\overline{\text{BOOT.SW.EN}}$ (Pin 9)
An active low input enabling the BOOT.SWAP output current pulse.

$\overline{\text{CS}}$ (Pin 7)
An active low input for selecting the chip. The chip powers down during deselect.

GEN.A (Pin 18)
An output providing the current pulse for writing data into the "A" quads of the bubble memory.

GEN.B (Pin 19)
An output providing the current pulse for writing data into the "B" quads of the bubble memory.

$\overline{\text{GEN.EN.A}}$ (Pin 5)
An active low input enabling the GEN.A output current pulse.

$\overline{\text{GEN.EN.B}}$ (Pin 4)
An active low input enabling the GEN.B output current pulse.

$\overline{\text{PWR.FAIL}}$ (Pin 21)
An active low output indicating that either V_{CC} or V_{DD} is less than 80% of its nominal value.

REFR. (Pin 20)
The pin for the reference current generator to which an external resistance must be connected.

REP.A (Pin 15)
An output providing the current pulse for replication of data in the "A"' quads of the bubble memory.

REP.B (Pin 16)
An output providing the current pulse for replication of data in the "B" quads of the bubble memory.

$\overline{\text{REP.EN}}$ (Pin 8)
An active low input enabling the REP.A and REP.B outputs.

SWAP (Pin 17)
An output providing the current pulse for exchanging the data between the input track and the storage loops in the bubble memory.

$\overline{\text{SWAP.EN}}$ (Pin 6)
An active low input enabling the SWAP output.

$\overline{\text{TM.A}}$ (Pin 2)
An active low timing signal determining the cut pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.

$\overline{\text{TM.B}}$ (Pin 3)
An active low timing signal determining the transfer pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.

7230

D.C. and Operating Characteristics

T_A=0°C to +70°C, V_{CC}=5.0V ±5%, V_{DD}=12V ±5%, unless otherwise specified.

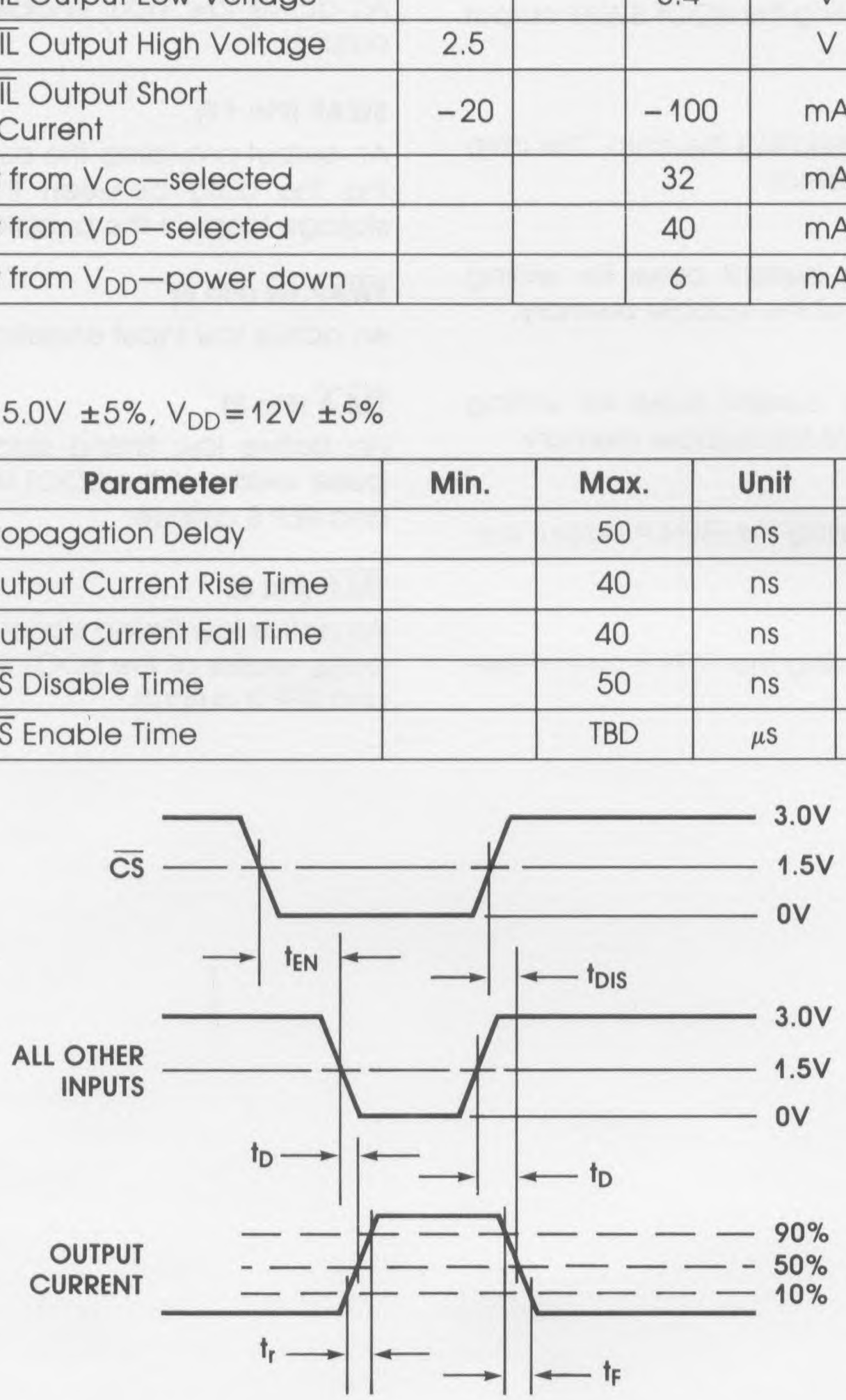
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{IL}	Input Low Current			−0.4	mA	V_{IL}=0.4V
I_{IH}	Input High Current			20	μA	V_{IH}=2.7V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_C	Input Clamp Voltage			−1.5	V	I= −18 mA
I_{CEX}	Output Leakage Current			1.0	mA	
V_{OL}	$\overline{\text{PWR.FAIL}}$ Output Low Voltage			0.4	V	I_{OL}=4 mA
V_{OH}	$\overline{\text{PWR.FAIL}}$ Output High Voltage	2.5			V	I_{OH}= −0.4 mA
I_{OS}	$\overline{\text{PWR.FAIL}}$ Output Short Circuit Current	−20		−100	mA	V_{CC}=5.5V
I_{CC1}	Current from V_{CC}—selected			32	mA	$\overline{CS}$=V_{IL}
I_{DD1}	Current from V_{DD}—selected			40	mA	$\overline{CS}$=V_{IL}
I_{DD2}	Current from V_{DD}—power down			6	mA	$\overline{CS}$=V_{IH}

A.C. Characteristics

T_A=0°C to +70°C, V_{CC}=5.0V ±5%, V_{DD}=12V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_D	Propagation Delay		50	ns	
t_r	Output Current Rise Time		40	ns	
t_F	Output Current Fall Time		40	ns	
t_{DIS}	$\overline{CS}$ Disable Time		50	ns	
t_{EN}	$\overline{CS}$ Enable Time		TBD	μs	

Waveforms



Capacitance*

T_A=25°C

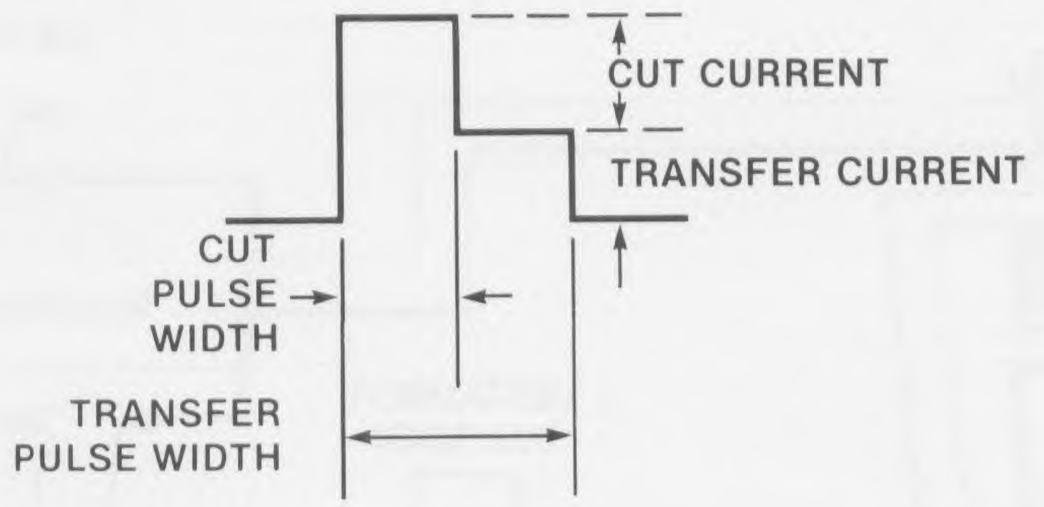
Symbol	Test	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	

*This parameter is periodically sampled and not 100% tested. Condition of measurement is f=IMHz, V_{bias}=2V.

Output Currents

Output (V_{OUT} =3.0V)	Nominal Values at 50 KHz		
	Current (mA)	Pulse Width (μs)	Duty Cycle (%)
REP.A, REP.B CUT	180	0.25	0.006
REP.A, REP.B TRANSFER	140	5.0	0.12
BOOT.REP CUT	TBD	0.25	1.3
BOOT.REP TRANSFER	TBD	0.25	1.3
GEN.A, GEN.B CUT	130	0.25	1.3
GEN.A, GEN.B TRANSFER	40	3.0	15
SWAP	140	30.0	0.8
BOOT.SWAP	TBD	*See Note	

Two-level pulses are defined as shown:



Note: Writing data into the bootstrap loop would require 4096 pulses of 20 μs width.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . −20°C to +80°C
Storage Temperature . . . . . −65°C to +150°C
V_{CC} and Input Voltages . . . . . −0.5V to +7V
V_{DD} and Output Voltages . . . . . −0.5V to +14V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Preliminary

7242
DUAL FORMATTER/SENSE AMPLIFIER FOR BUBBLE MEMORIES

Features

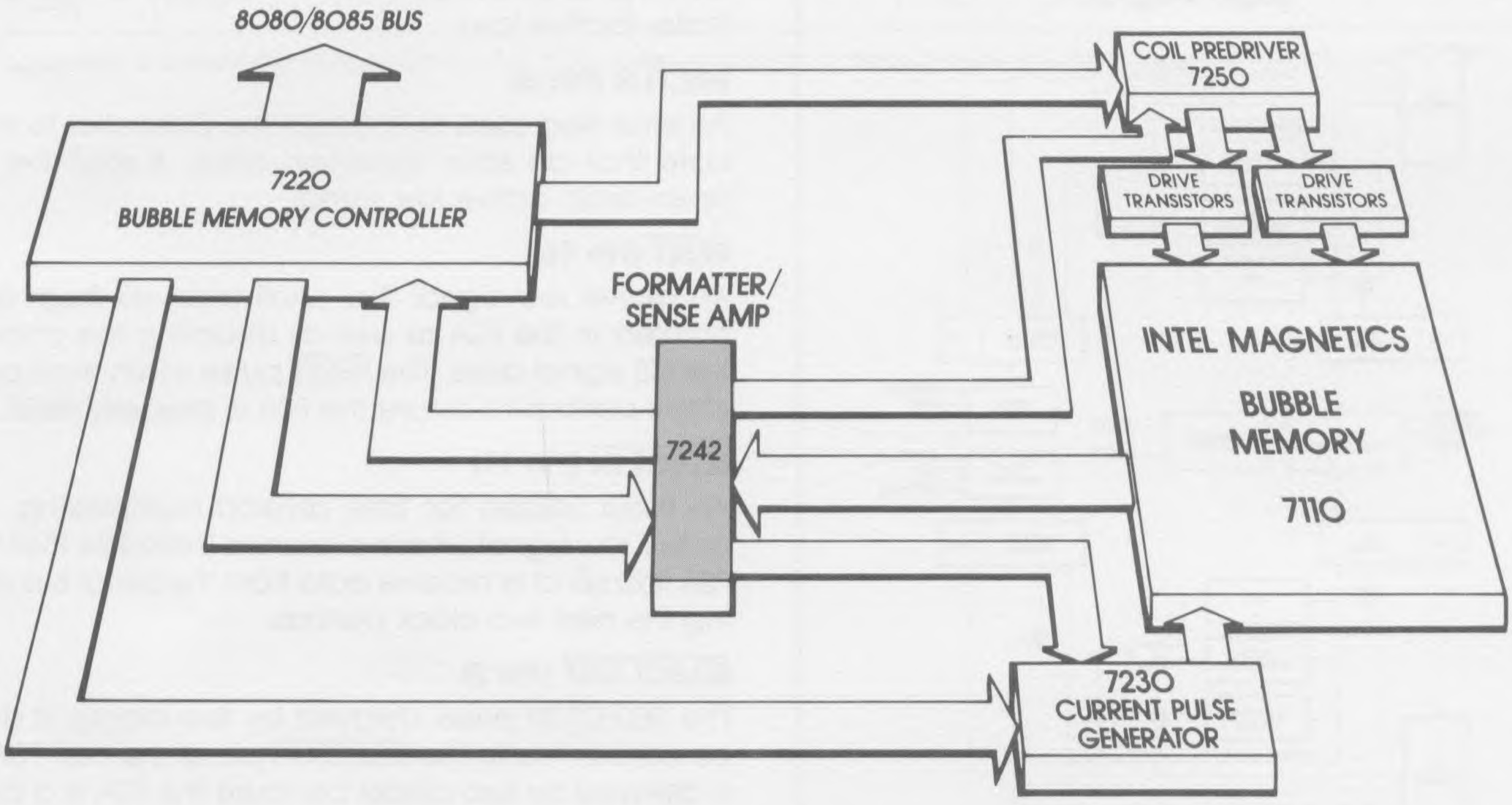
- **Ideal for Use with IM's Bubble Memories**
- **Dual Channel**
- **On-Chip Sense Amplifiers**
- **Automatically Handles Redundant Loops**
- **Error Detection/Correction done Automatically**
- **FIFO Data Block Buffer**
- **Daisy-Chained Selects for Multiple Bubble Memory Systems**
- **MOS N-Channel Technology**
- **Standard 20-Pin Dual In-Line Package**

Description

The Intel 7242 is a Dual Formatter/Sense Amplifier (FSA) designed to interface directly with Intel Magnetics Bubble Memories. The 7242 features on-chip sense amplifier for system ease of use and minimization of system part count. The 7242 also provides for automatically handling the bubble memories' redundant loops so they appear transparent to the user. In addition, complete burst error detection and correction can be done automatically by this device.

The 7242 has a full FIFO data block buffer. This device can be daisy-chained for multiple bubble memory systems. Up to eight FSA can be controlled by one 7220 Bubble Memory Controller (BMC).

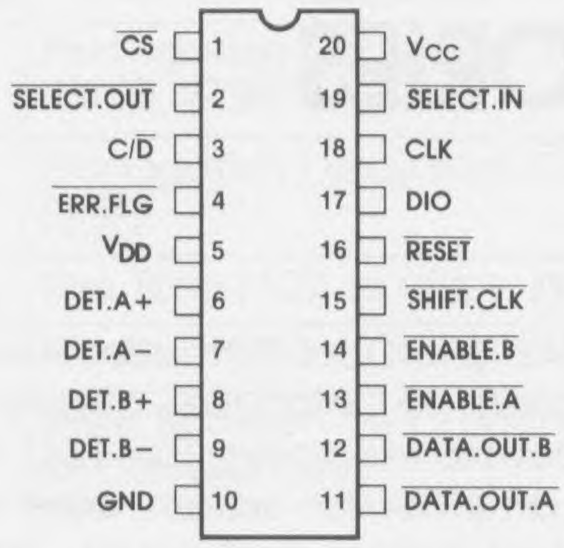
The 7242 utilizes an advanced NMOS technology to incorporate the on-chip sense amplifiers and other unique features. The device is packaged in a standard high density 20-pin dual in-line package.



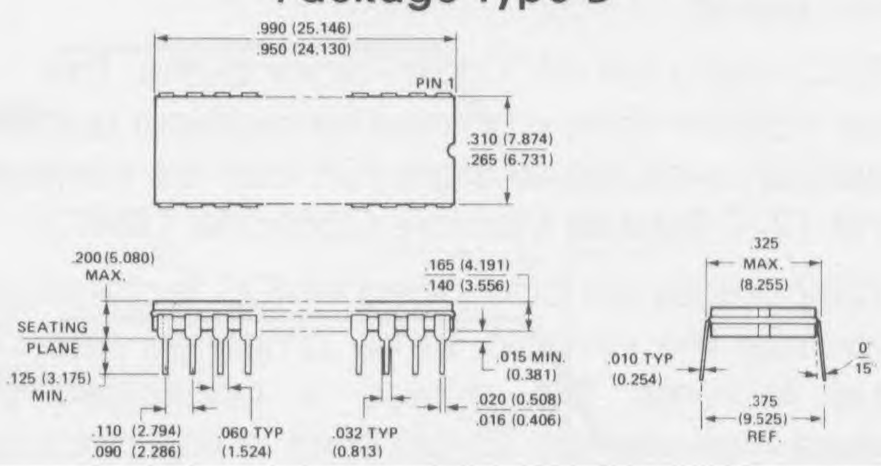
Block Diagram of Single Bubble Memory System — 128K Bytes

7242

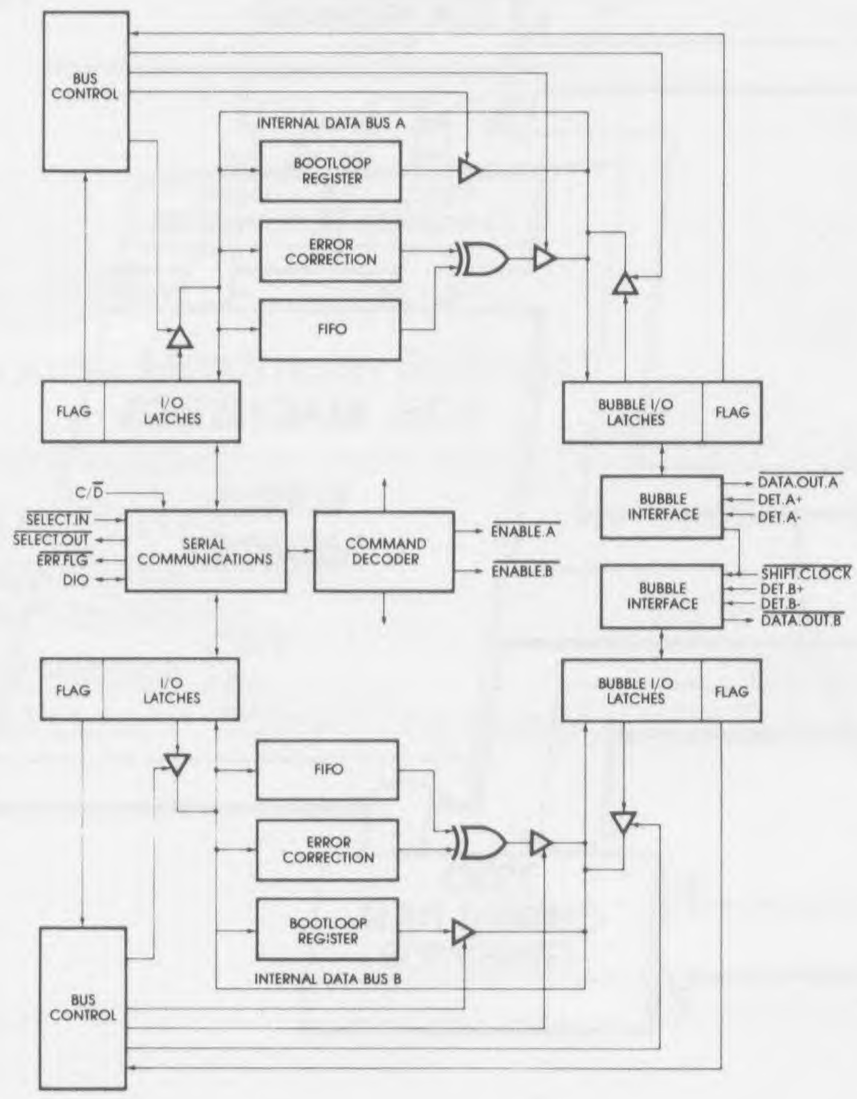
Pin Configuration



Packaging Information
20-Lead Hermetic Dual-In-Line
Package Type D



Logic Diagram



Pin Description

C/$\overline{D}$ (Pin 3)

Command/$\overline{Data}$ signal. This signal shall cause the FSA to enter a receive command mode when high and to interpret the serial data line as data when low. Any previously active command will be immediately terminated by C/$\overline{D}$.

CLK (Pin 18)

A 0.5 to 5 MHz, 50% ±10% duty cycle TTL level clock used to generate internal timing.

$\overline{CS}$ (Pin 1)

An active low signal used for multiplexing of FSA's. The FSA is disabled whenever $\overline{CS}$ is high (i.e., it presents a high impedance to the bus and ignores all bus activity.)

$\overline{DATA.OUT.A}$, $\overline{DATA.OUT.B}$ (Pins 11 and 12)

Output data from the FIFO to the MBM generate circuitry, used to write data into the bubble device (active low).

DET.A+, DET.A–, DET.B+, DET.B– (Pins 6, 7, 8 and 9)

Differential signal lines from the MBM detector.

DIO (Pin 17)

The Serial Bus data line (a bidirectional active high signal).

$\overline{ENABLE.A}$, $\overline{ENABLE.B}$ (Pins 13 and 14)

TTL level outputs utilized as chip selects for other interface circuits. They shall be set and reset by the Command Decoder under instruction of the Controller (active low).

$\overline{ERR.FLG}$ (Pin 4)

An error flag used to interrupt the Controller to indicate that an error condition exists. It shall be an open drain active low signal.

$\overline{RESET}$ (Pin 16)

An active low signal that shall reset all flags and pointers in the FSA as well as disabling the chip as the CS signal does. The $\overline{RESET}$ pulse width must be 5 clock periods to assure the FSA is properly reset.

$\overline{SELECT.IN}$ (Pin 19)

An input utilized for time division multiplexing. An active low signal whose presence indicates that the FSA is to send or receive data from the Serial Bus during the next two clock periods.

$\overline{SELECT.OUT}$ (Pin 2)

The $\overline{SELECT.IN}$ pulse delayed by two clocks. It shall be connected to the $\overline{SELECT.IN}$ pin of the next FSA. It is delayed by two clocks because the FSA is a dual channel device. Channel A shall internally pass $\overline{SELECT.IN}$ to Channel B (delayed by one clock).

Pin Description (Continued)

$\overline{\text{SHIFT.CLK}}$ (Pin 15)
A Controller generated clock signal that shall be used to clock data out of the bubble I/O Output Latch to the bubble module during a write operation and to cause bubble signals to be converted by the Sense Amp and clocked into the Bubble I/O Input Latch on a read.

Functional Description

The following is a brief description of each block of the 7242 FSA.

Serial Communications — The Serial Communications block handles all transfers on the Serial Bus and is shared by both channels of the FSA.

Command Decoder — The Command Decoder interprets commands by the Serial Communication logic and sets the appropriate command and enable lines. It also maintains FSA status, and generates various reset lines.

Internal Data Bus — The Internal Data Bus is the main data link between the Serial Communications block and all other data sources in each half of the FSA.

I/O Latches, Flags, and Bus Control — Each channel of the FSA has its own Internal Data Bus, on which all data transfers are made. There is a Flag and a bidirectional Latch in each "I/O Latches — Flag" block. Only one Latch is used in a given operation and the Flag tells the Bus Controller whether or not the Latch is full. The Bus Controller monitors these flags, and other control signals, to determine when each device should have access to the Internal Data Bus. When a transfer is to be made, the appropriate devices are enabled, the Bus is enabled, and the transfer takes place synchronously by virtue of a transparent State Machine Sequencer.

FIFO — The FIFO is a variable length First-In-First-Out buffer utilized to store data passing to and from the MBM module. The FIFO is logically 272 bits in length in the "no error correction" mode. It is 270 bits in the "error correction" mode, since 256 bits of data and a 14 bit error correction code must be used in this mode of operation.

The FIFO pointers are reset by hardware or software resets or each time a command to read or write is received by the Command Decoder.

If a block length other than 272 bits is used in the no error correction mode, the FIFO pointers will not return to word zero at the end of each block transfer. This is of no consequence if one is not concerned about the absolute location of data in the FIFO. Keeping in mind that the FIFO is only 272 bits physically, any block length may be used up to and including 320.

Bootstrap Loop Register — The Bootstrap Loop Register is a 160 bit register that contains information detailing the location of bad loops in the MBM module. This data will enable FIFO I/O to ensure that bits are not loaded in the FIFO from bad loops, or written from the FIFO into bad loops. A logic zero (absence of a bubble) is written into bad loops.

Error Correction Logic — The Error Correction Logic contains the circuitry to implement a burst error correcting code capable of correcting any single burst error of length equal to or less than 5, anywhere in the 270 bit data stream, including the error correction code which is 14 bits in length. A Correction Enable bit may be set or reset via a special command. When reset, the entire error correction network is disabled and block length may vary from 270 bits. Error detection shall be accomplished on all data transfers (when enabled); however, correction cannot take place unless the FSA is operated in a buffered mode (i.e., an entire block is read prior to passing any data to the Controller).

Bubble I/O — The Bubble I/O consists of an integrated Sense Amplifier and an output driver. The Sense Amplifier consists of a sample-and-hold circuit and a differential, chopper stabilized comparator.

Enables — The $\overline{\text{ENABLE.A}}$ and $\overline{\text{ENABLE.B}}$ outputs are utilized as chip selects for external circuitry. To set an ENABLE line, the desired channel of the FSA must be selected and a Read or Write MBM, Set Enable Bit, Initialize, Read Collected Data, or Internally Correct Data command is sent. Any other command sequence will reset the ENABLE lines.

Commands

FSA Commands — The FSA shall receive a four bit command word via the Serial Bus. In addition, some of the commands require additional data bits, e.g., status to be passed.

Commands (Continued)

serially. The four bits shall be interpreted as shown in Table 1. The effects on the Status bits, Correction Enable bit, and Enable pins are summarized in Table 2.

The following is a brief description of each command available in the 7242 FSA.

No Operation — Deselects the chip and prevents further internal activity (default state for reset, unselected or unaddressed channels). Resets the FIFO and Bootloop pointers. The Enable pins (ENABLE.A and ENABLE.B) become inactive.

Software Reset — Resets all FIFO and Bootloop pointers and flags. Status flags, Error Correction Enable bit, error correction shift register, and the Enable pins become inactive.

Initialize — The chip is set to read data from the MBM Bootloop and pass it to the Controller. Resets

Table 1
Command Code Descriptions

Code	Description	Data	
		Correction Enabled	Not Enabled
0000	No operation	None	None
0001	(Reserved)	—	—
0010	Software Reset	None	None
0011	Initialize	MBM Bootloop	MBM Bootloop
0100	Write MBM Data	270 Bits In	Variable
0101	Read MBM Data	270 Bits Out	Variable
0110	Internally Correct Data	None	—
0111	Read Corrected Data	270 Bits Out	—
1000	Write Bootloop Register	160 Bits In	160 Bits In
1001	Read Bootloop Register	160 Bits Out	160 Bits Out
1010	(Reserved)	—	—
1011	(Reserved)	—	—
1100	Set Enable Bit	None	None
1101	Read $\overline{\text{ERR.FLG}}$ Status	1 Bit Out	1 Bit Out
1110	Set Correction Enable Bit	None	None
1111	Read Status Register	8 Bits Out	8 Bits Out

Table 2
Command Function Summary

Command Description	Command Code	Data Flow (R/W)	Reset FIFO & Bootloop Pointers	Reset Status (Errors)	Reset Error Correction Logic	Enable
No Operation	0000	—	X			H
Software Reset	0010	—	X	X	X	H
Initialize	0010	R	X	X	X	L
Write MBM Data	0100	W	X		X	L
Read MBM Data	0101	R	X		X	L
Internally Correct Cata	0110	—	X			L
Read Corrected Data	0111	R	X			L
Write Bootloop Register	1000	W	X			H
Read Bootloop Register	1001	R	X			H
Set Enable Bit	1100	—	X			L
Read $\overline{\text{ERR.FLG}}$ Status	1101	R	X			H
Set Error Correction Enable Bit	1110	—	X			H
Read Status Register	1111	R	X	X		H

Commands (Continued)

the FIFO and Bootloop pointers, Error Correction Logic, and disables the Bootloop register, (so that it does not interfere with the data flow). The Enable pins become active in addressed channels.

Write MBM Data — Data input by the Controller is written into the good loops in use in the MBM (under control of the Bootloop register) each time a $\overline{\text{SHIFT.CLK}}$ is received. It also activates the Enable pins and resets the FIFO and Bootloop pointers. If the Correction Enable bit is set, the FSA computes the correction code and appends it to the data stream to be stored in the MBM (last 14 of 270 bits).

Read MBM Data — This command activates the ENABLE pins and resets the FIFO and Bootloop pointers independent of the state of the Correction Enable bit. If the Correction Enable bit is reset, data, of block length dictated by 2 times the number of logic '1's in the Bootloop register, from the MBM is sensed and screened by the FSA Sense Amp and Bootloop register, and stored in the FIFO. As soon as one bit is guaranteed in the FIFO, simultaneous reading from the FIFO may be done by the Controller. The FIFO need not be emptied after each page is read, but one must insure that more than 272 bits of FIFO are not needed at any time during the transfer.

If the Correction Enable is set; data must be read in a buffered mode. First, a full block of data is read from the MBM. At that point the FIFO contains 270 bits of data. If an error is detected by the Error Correction network, the FSA raises the UNCORR.ERR and CORR.ERR flags which generate an interrupt to the controller. If no error is detected, the 270 bits of data may be read from the FIFO while sumultaneously reading and checking the next block of data from the MBM. When an error is detected the Controller may respond to the interrupt in one of 3 ways.

(1) Ignore it and try again (must make sure to reset the Error Correction shift register before a retry).

(2) Send a Read Corrected Data command to the FSA. This command will correct the data stream (if possible) and interrupt the Controller when the block has been read. At this time the Controller can send a Read Status command to see if the error was correctable (CORR.ERR) or uncorrectable (UNCORR.ERR).

(3) Send an Internally Correct Data command to the FSA. The FSA corrects the data without transferring it to the Controller. When finished, the FSA interrupts the Controller. At this point it can be determined whether or not the error is correctable. If so, a Read Corrected Data command may be sent to read the good data.

Internally Correct Data — Internally cycles the data through the error correction network and returns status as to whether or not the data is correctable.

Requires approximately 1400 clock cycles to complete. $\overline{\text{ERR.FLG}}$ will be inactive during internal cycling, but will return active at its completion. Also activates the ENABLE pins and resets the FIFO and Bootloop pointers.

Read Corrected Data — Cycles data through the error correction network with each Controller read (SELECT.IN at the FSA). At the end of 270 reads, status is available to indicate whether or not the data was successfully corrected. $\overline{\text{ERR.FLG}}$ acts as in Internally Correct Data. This command is required to read data corrected internally as well, but has no effect on the data read if it was successfully corrected. Activates the ENABLE pins and resets the FIFO and Bootloop pointers.

Write Bootloop Register — Contents of the FSA's Bootloop register are written with 160 bits from the Controller. The Controller must read the MBM Bootloop first, to determine which loops are good. The number of good bits in the 160 bit register is 135 if correction is used, and variable up to 160 if operating in the no correction mode. ENABLE pins become inactive and the FIFO and Bootloop pointers are reset.

Read Bootloop Register — As above except that data is read from the FSA Bootloop to the Controller.

Set Enable Bit — ENABLE pins become active for addressed channels, inactive for unaddressed channels. Also resets the FIFO and Bootloop pointers.

Read $\overline{\text{ERR.FLG}}$ Status — Reads the composite error status for addressed channels of the FSA. (The composite status is the logic OR of CORR.ERR, UNCORR.ERR and TIMER.R). The $\overline{\text{ERR.FLG}}$ pin is the logic NOR of both channels composite error status; ERR.FLG.A and ERR.FLG.B.) ENABLE pins become inactive and FIFO and Bootloop pointers are reset.

Commands (Continued)

Set Error Correction Enable Bit — Enables the Error Correction Logic in addressed FSA's and disables it in unaddressed FSA's. ENABLE pins become inactive and FIFO and Bootloop pointers are reset. Furthermore, when this enable is set, the corresponding FIFO becomes a 270 bit FIFO (logically) instead of a 272 bit FIFO as in the no correction mode.

Read Status Register — The 8 bit Status Word for the addressed FSA is output to the Controller. Only one FSA channel can be addressed at a time, or bus contention may result. ENABLE pins become inactive and error flags in the addressed FSA channel, and FIFO and Bootloop pointers are reset.

Serial Interface

Command Sequence — The FSA communicates with the Controller via a Serial Interface. The Controller/FSA Interface contains the following signals.

(1) CLK
(2) $\overline{\text{SELECT.IN}}$ (Formatter)
(3) $\overline{\text{SELECT.OUT}}$ (Formatter)
(4) $\overline{\text{SYNC}}$ (Controller)
(5) DIO
(6) C/$\overline{\text{D}}$
(7) $\overline{\text{SHIFT.CLK}}$
(8) $\overline{\text{ERR.FLG}}$

Commands from the Controller to the FSA shall take place in the following format (see Figure 1).

(1) Controller raises C/$\overline{\text{D}}$ flag indicating that a command is coming, and simultaneously outputs a SYNC pulse. This SYNC pulse is shifted down the FSA chain in shift register fashion via the FSA $\overline{\text{SELECT.IN}}$/$\overline{\text{SELECT.OUT}}$ lines.

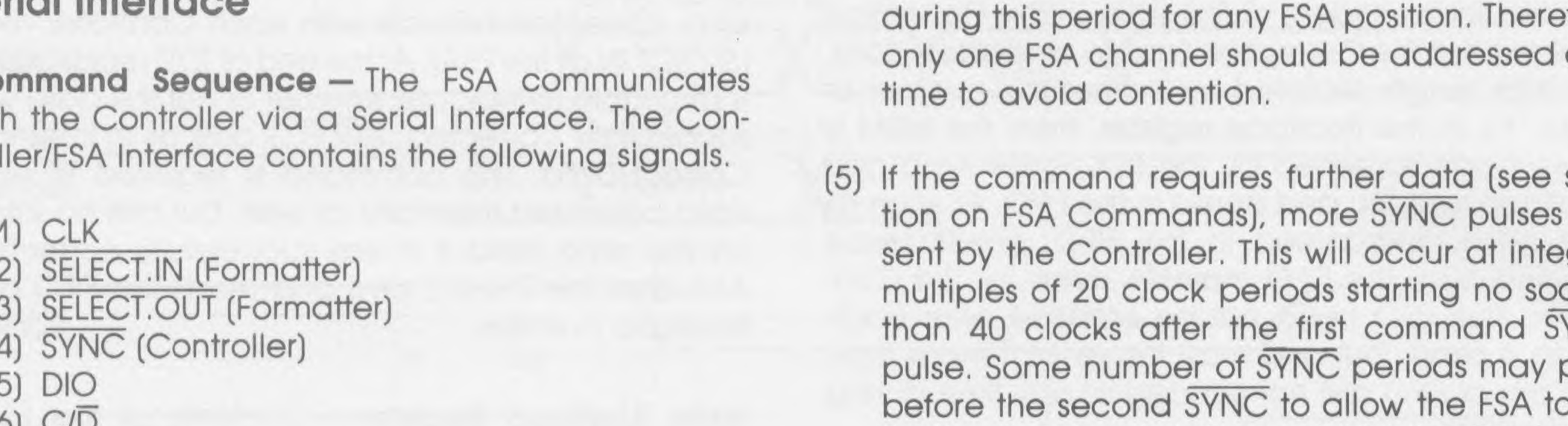
(2) Controller outputs a serial data stream on the DIO line beginning in the clock period following SYNC. Each bit in the stream corresponds to an address bit for a particular FSA (up to 16 channels). Each FSA, upon receiving $\overline{\text{SELECT.IN}}$, will look for the presence or absence of a logic one on DIO in the clock period following receipt of $\overline{\text{SELECT.IN}}$ (a logic one indicates that the FSA shall accept the command).

(3) Twenty clock periods after the first $\overline{\text{SYNC}}$, the Controller sends C/$\overline{\text{D}}$ low followed by a four bit command on the DIO line.

(4) If the command is a Read Status command (1111), the addressed FSA returns 8 bits of Status starting 4 clock periods after the last command bit is received. Note that the Status is returned during this period for any FSA position. Therefore only one FSA channel should be addressed at a time to avoid contention.

(5) If the command requires further data (see section on FSA Commands), more $\overline{\text{SYNC}}$ pulses are sent by the Controller. This will occur at integral multiples of 20 clock periods starting no sooner than 40 clocks after the first command $\overline{\text{SYNC}}$ pulse. Some number of $\overline{\text{SYNC}}$ periods may pass before the second $\overline{\text{SYNC}}$ to allow the FSA to set itself up and get data ready for the Controller. There are several possibilities:

(a) For the Read $\overline{\text{ERR.FLG}}$ Status command the second $\overline{\text{SYNC}}$ can occur 40 clocks after the first $\overline{\text{SYNC}}$. This $\overline{\text{SYNC}}$ (or $\overline{\text{SELECT.IN}}$) causes each addressed FSA to send the appropriate Status information. No further $\overline{\text{SYNC}}$'s (without C/$\overline{\text{D}}$ high) should be sent.



NOTE: STATUS INFO IS ONLY PRESENT ON BUS FOR THE READ STATUS COMMAND SEQUENCE.

Figure 1. Command Sequences

Serial Interface (Continued)

(b) For the Read MBM Data (or Initialize) command the second $\overline{\text{SYNC}}$ must wait the appropriate number of $\overline{\text{SHIFT.CLOCK}}$'s to assure that valid data is available in the FIFO.

After this wait, each addressed FSA channel sends one bit of data on the DIO line for each $\overline{\text{SYNC}}$ (or $\overline{\text{SELECT.IN}}$) pulse.

(c) For the Read Bootloop Register command, the second $\overline{\text{SYNC}}$ can occur 60 clock cycles after the first $\overline{\text{SYNC}}$. The data transfer then proceeds as in (b).

(d) For the Write MBM Data or Write Bootloop commands, the DIO line is used to transfer data to the FSA on successive SYNC pulses. The first data bit can be transferred by a second $\overline{\text{SYNC}}$ pulse, 40 clock cycles after the first $\overline{\text{SYNC}}$. (However, data to the MBM will not be available at the Dataout pins until 40 clock cycles after the $\overline{\text{SYNC}}$ which transferred it.) Each transfer to the addressed FSA will be initiated by a $\overline{\text{SYNC}}$ (or $\overline{\text{SELECT.IN}}$).

(6) $\overline{\text{SYNC}}$ ($\overline{\text{SELECT.IN}}$) precedes the data it transfers by 1 clock cycle. Data Transfers to or from the FSA's FIFO must contain the proper number of $\overline{\text{SYNC}}$'s (externally counted) or a timing error may occur ($\overline{\text{TIMERR}}$ flag will be set, causing an interrupt to the Controller).

Data Sequences — Bubble data shall be passed between the Controller and FSA's in the following fashion (see Figure 2).

(1) Controller outputs a $\overline{\text{SYNC}}$ pulse.

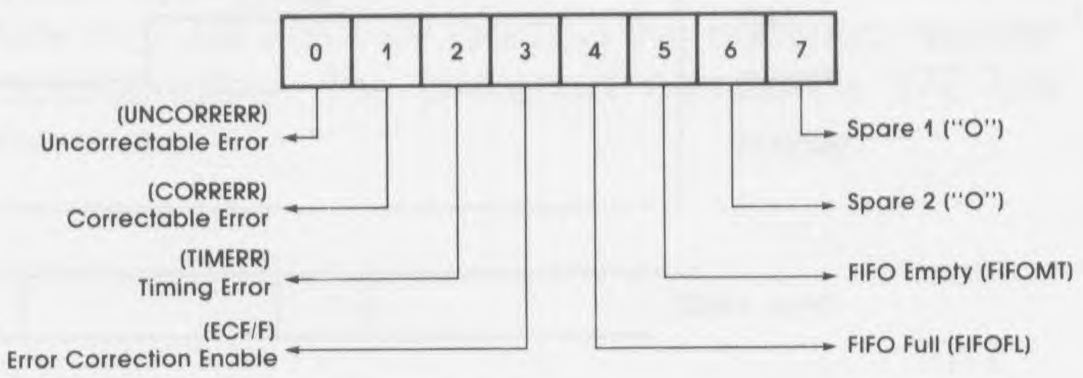
(2) Each FSA then outputs (inputs) a single bit on DIO after $\overline{\text{SYNC}}$ ($\overline{\text{SELECT.IN}}$) has been clocked into its control section. Only previously enabled FSA's output (input) data and the Controller must know when to input (output) data bits.

(3) After 20 clocks, another $\overline{\text{SYNC}}$ pulse is output and the sequence repeats until all data has been transferred.

Error Conditions — Each FSA shall upon detection of an error set a Status bit and pull down $\overline{\text{ERR.FLG}}$. This signal can be asynchronous to $\overline{\text{SYNC}}$. Error Status bits shall be:

(1) Correctable Error
(2) Uncorrectable Error
(3) Timing Error

The Status Word that shall be passed to the Controller after receipt of a Read Status command shall be in the following format:



NOTE: ERROR FLAGS SHALL BE RESET UPON BEING READ BY THE CONTROLLER OR BY A SOFTWARE RESET.

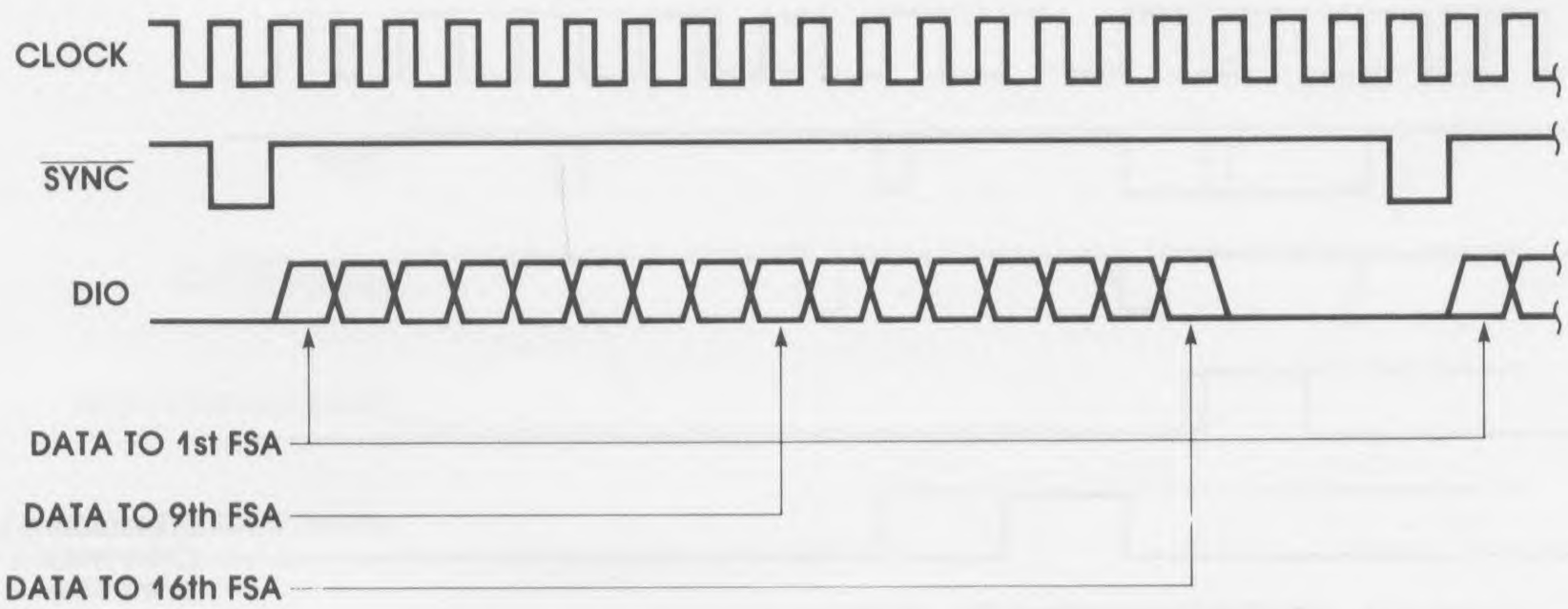


Figure 2. Data Sequences

Bubble Interface

Bubble Interface — Each Bubble Interface shall consist of a DATAOUT signal and a pair of differential inputs from the MBM detector bridge.

Read Timing — The timing for reading a bit from the memory shall be as follows (see Figure 3):

(1) Controller outputs a $\overline{\text{SHIFT.CLK}}$. FSA samples bubble signal during $\overline{\text{SHIFT.CLK}}$ and holds signal after trailing edge.

(2) Trailing edge of $\overline{\text{SHIFT.CLK}}$ initiates signal conversion timing.

(3) Data is latched at end of conversion period in the Bubble Input latch, and will subsequently be loaded into the FIFO.

Write Timing — The timing for writing a bit from the FIFO shall be as follows (see Figure 4):

(1) Controller lowers $\overline{\text{SHIFT.CLK}}$.

(2) Data is gated out of FSA by $\overline{\text{SHIFT.CLK}}$.

(3) Controller outputs a generate pulse (to external logic; not to FSA).

(4) Controller raises $\overline{\text{SHIFT.CLK}}$. The $\overline{\text{DATA.OUT}}$ pin is forced high.

(5) FIFO and Bootloop register are incremented after the trailing edge of $\overline{\text{SHIFT.CLK}}$.

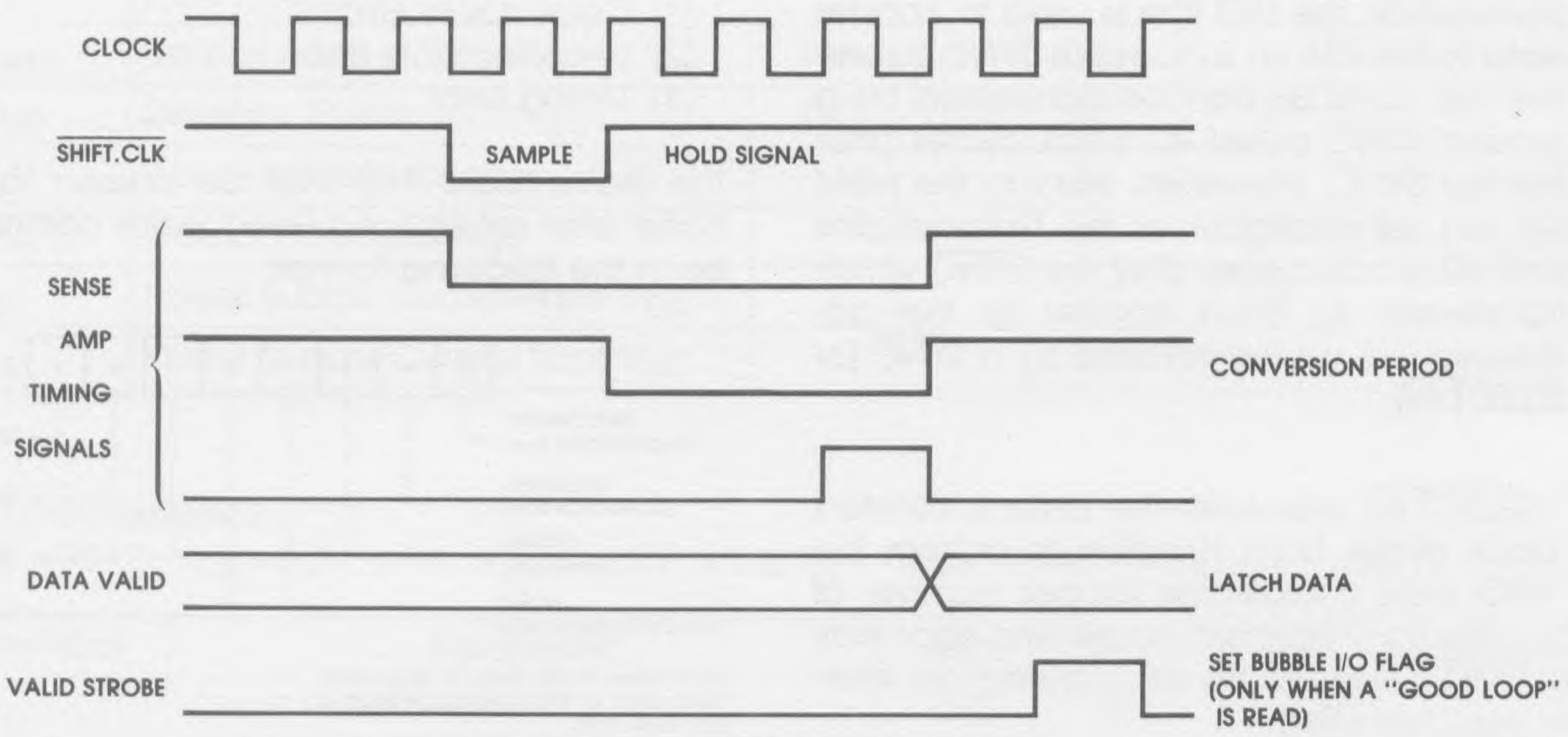


Figure 3. Data Read Timing

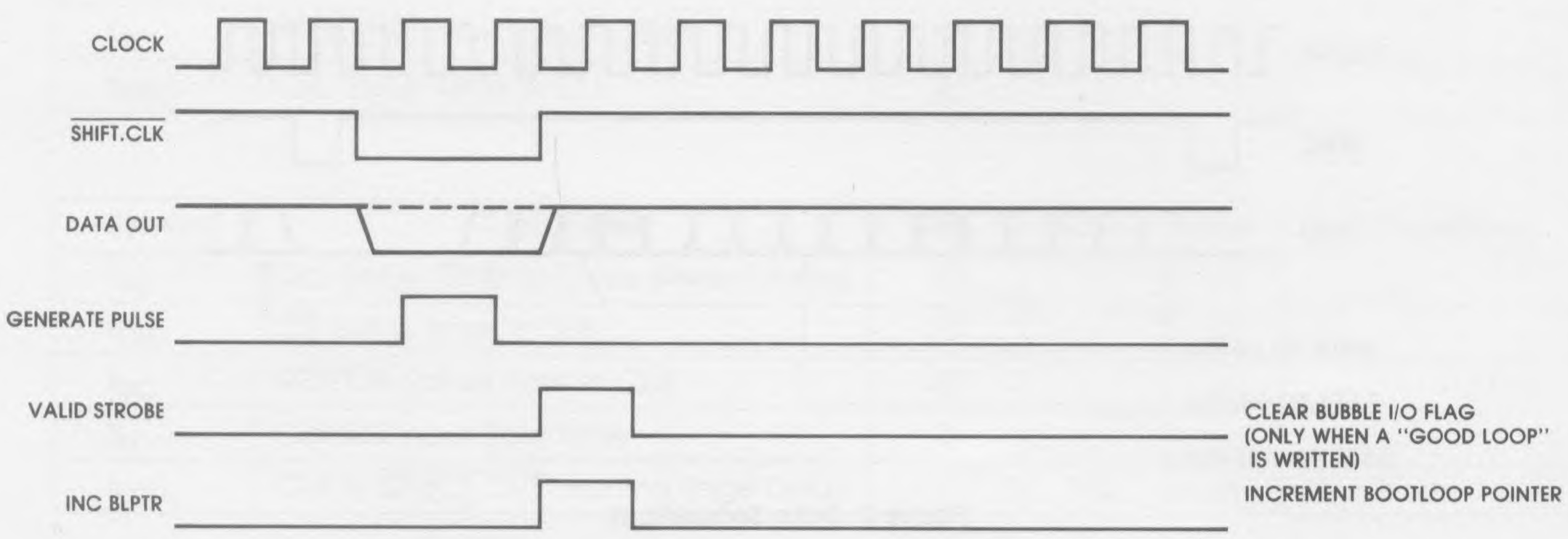


Figure 4. Write Timing

Bubble Interface (Continued)

System Timing — The $\overline{\text{SYNC}}$ pulse (which denotes the beginning of a data transfer from Controller to Formatter or vice-versa) shall be synchronous with the beginning of a bubble memory field rotation. Due to timing constraints in the FSA, the following statements hold:

(1) Data read from the bubble memory into the FSA shall not be available to the Controller until two field rotations after $\overline{\text{SHIFT.CLK}}$.

(2) Data cannot be written to the bubble memory until two field rotations after $\overline{\text{SYNC}}$ (see Figure 5).

FSA Error Correction

Error Correction — The error correction logic consists of a burst error correcting Fire code capable of correcting 5 or less bits in a single burst, the number of check bits is 14.* Error correction/detection shall take place on each 256 bit data block. The FSA shall drop $\overline{\text{ERR.FLG}}$ each time a correctable or uncorrectable error is detected. $\overline{\text{ERR.FLG}}$ shall be set upon being read by the Controller or by a software reset being issued. The polynominal implemented is given below:

$$G(X) = 1 + X^2 + X^5 + X^9 + X^{11} + X^{14}$$

*See "Error-Correcting Codes" by W. W. Peterson and E. J. Weldon, Jr., pp. 366–370, M.I.T. Press, 1972.

Data Format

Data Format — Data into the FSA from the bubble memory shall be in the format described below. The following definitions apply:

o_η = data from odd half of bubble device, loop η
e_η = data from even half of bubble device, loop η

Data Block Format:

$$o_1e_1o_1e_1o_2e_2o_2e_2 \ldots o_{80}e_{80}o_{80}e_{80}$$

1st bit 320th bit

When using correction, the first 270 good bits will be used, the last 14 of these are to be used for the error correcting code. The remaining 50 bits must be masked as "bad" bits in the FSA Bootloop register.

When operating without correction, any number of bits may be used by loading the Bootloop register appropriately. The preferred number is 272 bits however.

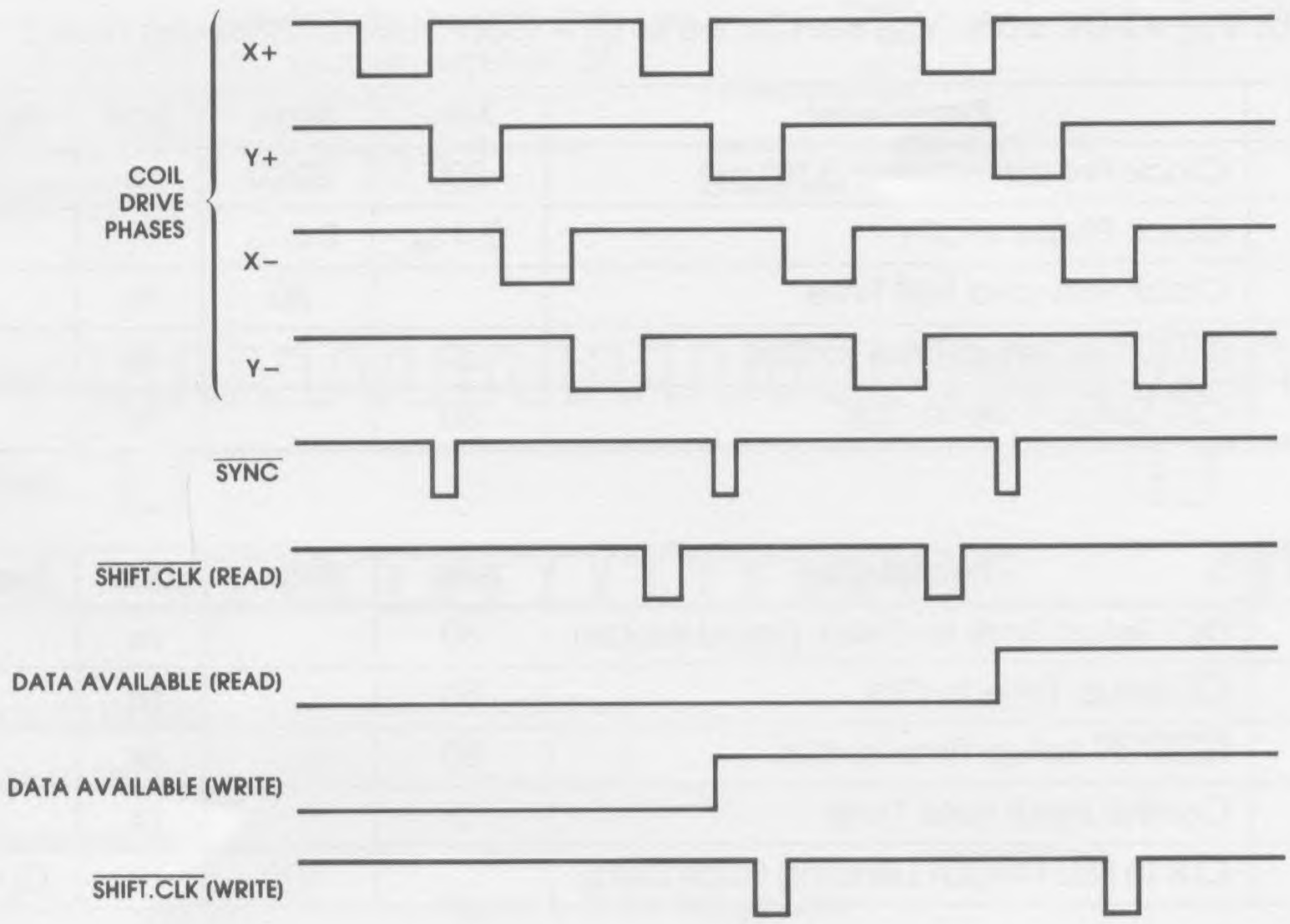


Figure 5. System Timing

D.C. and Operating Characteristics

T_A=0°C to +70°C, V_{CC}=5.0V ±5%, V_{DD}= +12V ±5%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+ 0.5	V	
V_{OL}	Output Low Voltage (All Outputs except $\overline{\text{SELECT.OUT}}$)			0.45	V	I_{OL}=3.2 mA
V_{OLSO}	Output Low Voltage ($\overline{\text{SELECT.OUT}}$)			0.45	V	I_{OL}=1.6 mA
V_{OH}	Output High Voltage (All Outputs except $\overline{\text{SELECT.OUT}}$)	2.4			V	I_{OH}=400 μA
V_{OHSO}	Output High Voltage ($\overline{\text{SELECT.OUT}}$)	2.4			V	I_{OH}=200 μA
V_{BIAS}	Detector Bias Voltage	TBD	6.0	TBD	V	
V_{THR}	Detector Threshold	TBD	0.004	TBD	V	
$\|I_{IL}\|$	Input Leakage Current			10	μA	$0 \le V_{IN} \le V_{CC}$
$\|I_{OFL}\|$	Output Float Leakage			10	μA	$0.45 \le V_{OUT} \le V_{CC}$
I_{CC}	Power Supply Current from V_{CC}			120	mA	
I_{DD}	Power Supply Current from V_{DD}			30	mA	

A.C. Characteristics

T_A=0°C to +70°C, V_{CC}=5.0V ±5%, V_{DD}= +12V ±5%, C_L=150pF, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_p	Clock Period	200	2000	ns	
t_ϕ	Clock Phase Width	0.4 t_p	0.6 t_p		
t_r, t_f	Clock Rise and Fall Time		30	ns	
t_{SIC}	$\overline{\text{SELECT.IN}}$ Setup Time to CLK	50		ns	
t_{CDC}	C/$\overline{\text{D}}$ Setup Time to CLK	50		ns	

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{DC}	DIO Setup Time to Clock (Read Mode)	50		ns	
t_{CSC}	$\overline{\text{CS}}$ Setup Time to CLK	50		ns	
t_{RIC}	$\overline{\text{RESET.IN}}$ Setup Time to CLK	50		ns	
t_{IH}	Control Input Hold Time	0		ns	
t_{CSOL}	CLK to $\overline{\text{SELECT.OUT}}$ Leading Edge Delay		100	ns	C_L=50 pF

A.C. Characteristics (Continued)

T_A=0°C to +70°C, V_{CC}=5.0V ±5%, V_{DD}=+12V ±5%, C_L=150pF, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CSOT}	CLK to $\overline{\text{SELECT.OUT}}$ Trailing Edge Delay		80	ns	C_L=50 pF
t_{CDV}	CLK to DIO Valid Delay*		100	ns	
t_{CDH}	CLK to DIO Hold Time*	0		ns	
t_{CDE}	CLK to DIO Enabled from Float*		100	ns	
t_{SIDE}	$\overline{\text{SELECT.IN}}$ Trailing Edge to DIO Enabled from Float*	TBD	70	ns	

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CDF}	CLK to DIO Entering Float*		100	ns	C_L(DIO)=50 pF, I_{OL}=3.2 mA
t_{DFSO}	DIO Float to $\overline{\text{SELECT.OUT}}$ Trailing Edge	TBD		ns	C_L(DIO, $\overline{\text{SELECT.OUT}}$)=50 pF, I_{OL}=3.2 mA
t_{CEF}	CLK to $\overline{\text{ERR.FLG}}$ Delay		300	ns	R_L=1.6K to V_{CC}
t_{CEN}	CLK to $\overline{\text{ENABLE.A,B}}$		300	ns	

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{SCDO}	$\overline{\text{SHIFT.CLK}}$ to DATAOUT Delay*		200	ns	
t_{SCRV}	$\overline{\text{SHIFT.CLK}}$ Recovery Time	TBD		ns	
t_{SKEW}	$\overline{\text{SHIFT.CLK}}$ to Sample Skew		TBD	ns	
t_{SCW}	$\overline{\text{SHIFT.CLK}}$ Width	t_p		ns	

*Write Mode

Capacitance

T_A=25°C, V_{CC}=0V, f = 1 MHz

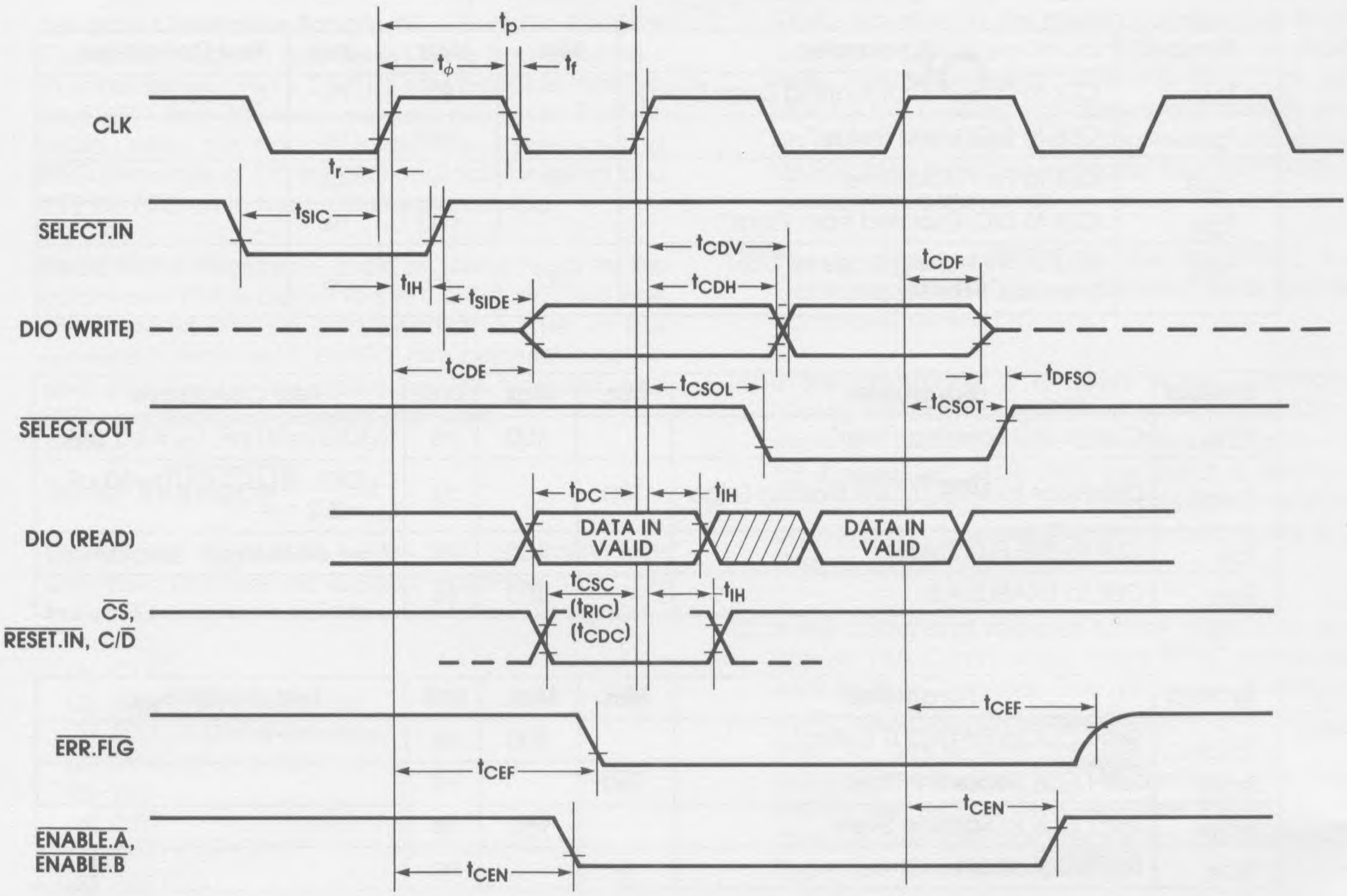
Symbol	Test	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	
C_{DIO}	DIO Capacitance		10	pF	

Absolute Maximum Ratings*

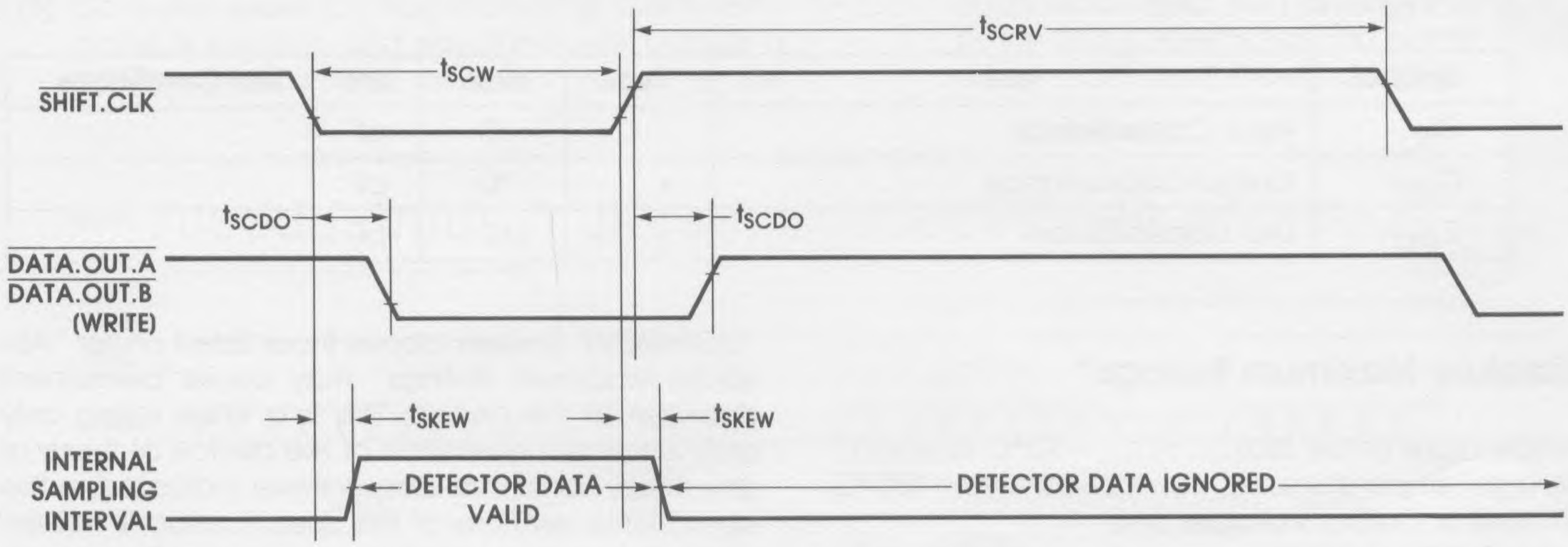
Temperature Under Bias . . . . . −10°C to +80°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages and
V_{CC} Supply Voltage . . . . . −0.5V to +7V
V_{DD} Supply Voltage . . . . . −0.5V to +14V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DIO INTERFACE TIMING



BUBBLE DATA INTERFACE TIMING



intel® magnetics

Preliminary

7250
COIL PRE-DRIVER FOR BUBBLE MEMORIES

Features

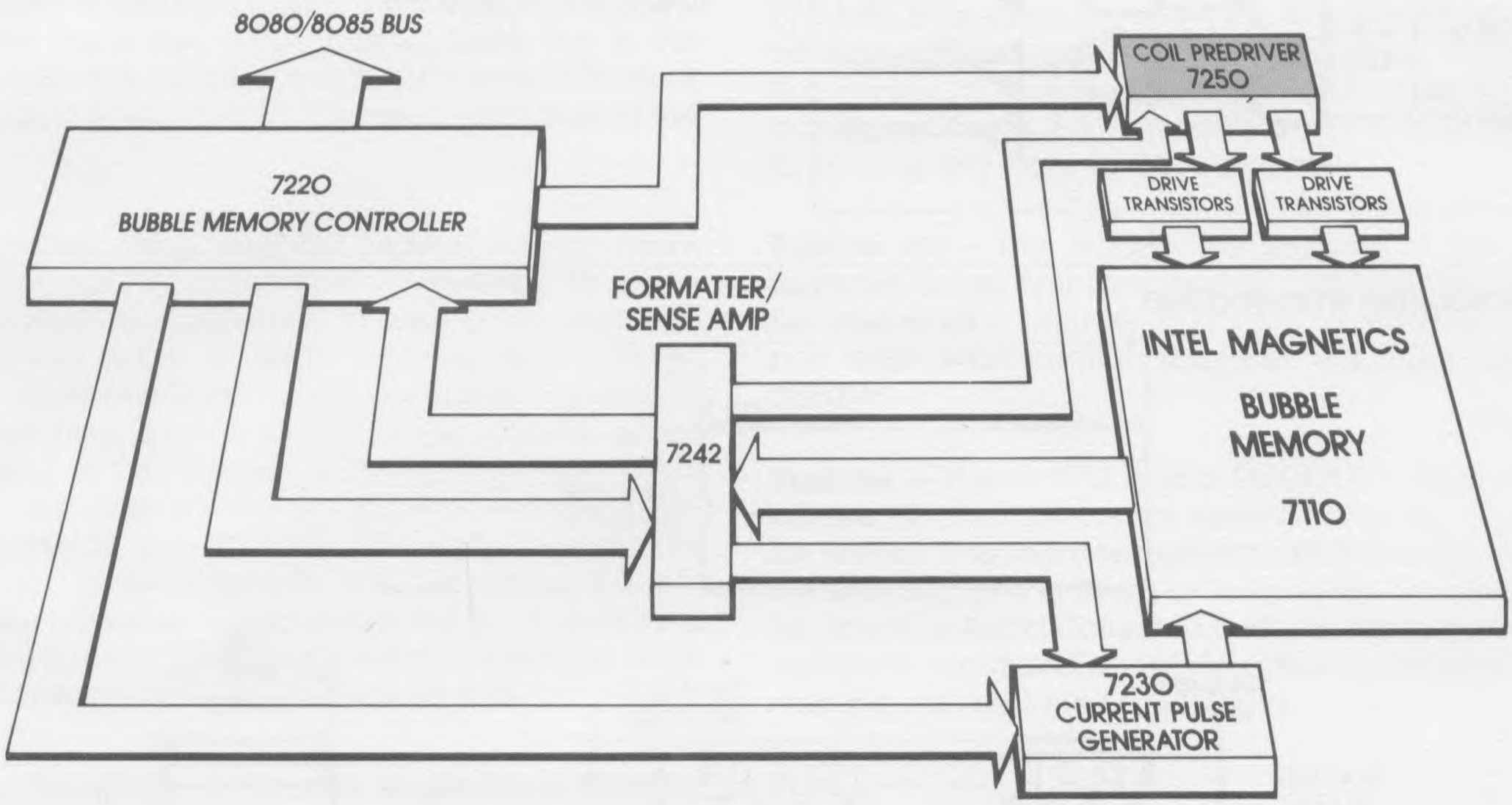
- **Ideal for Use with IM's Bubble Memories**
- **Very Low Power**
- **Power Fail Reset for Maximum Protection of Bubble Memory**
- **TTL Compatible Inputs**
- **Only One Power Supply Required, +12V**
- **CMOS Technology**
- **Standard 16-Pin Dual In-Line Package**

Description

The Intel 7250 is a low power Coil Pre-Driver (CPD) for use with Intel Magnetics Bubble Memories. The 7250 is controlled by the Intel 7220 Bubble Memory Controller (BMC) and directly drives either Quad VMOS transistor packs or Quad Bipolar transistor packs which are connected to the coils of the bubble memory.

The 7250 is a high voltage, high current driver constructed using CMOS technology. The device has TTL compatible inputs and the outputs are designed to drive either low on-resistance VMOS transistors or bipolar transistors.

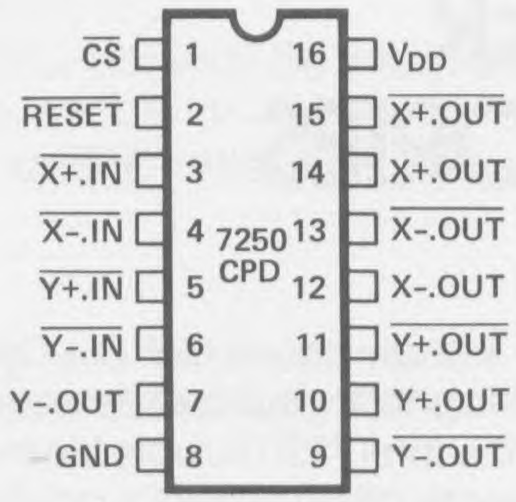
The 7250 is in a standard 16-pin dual in-line package.



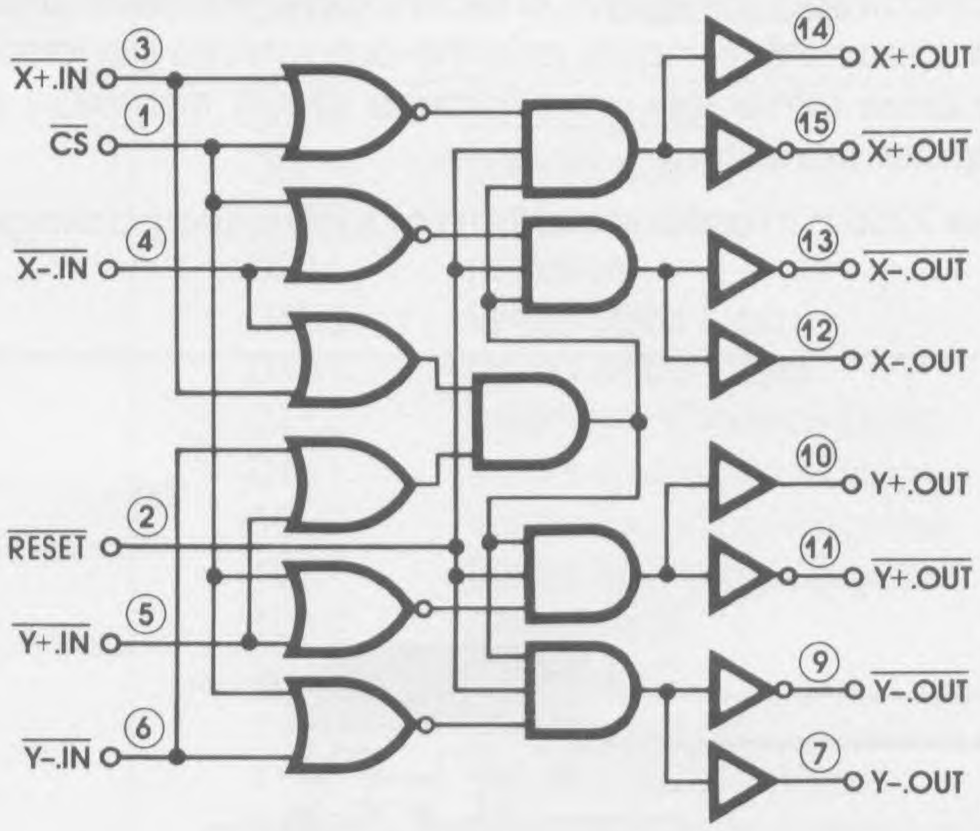
Block Diagram of Single Bubble Memory System — 128K Bytes

7250

Pin Configuration



Logic Diagram



Pin Description

CS (Pin 1)

Chip select. It is active low. When high chip is deselected and I_{DD} is significantly reduced.

RESET (Pin 2)

Active low input from RESET.OUT of 7220 Controller results in removal of power from the chip so that bubble memory is protected in the event of power supply failure.

X+.IN, X—.IN (Pins 3, 4)

Active low inputs from controller which turn on the high current X outputs.

X—.OUT, X—.OUT, X+.OUT, X+.OUT (Pins 12-15)

High current outputs and their complements for driving the gates of the 7254 VMOS quad transistors which in turn drive the X coils of the bubble memory.

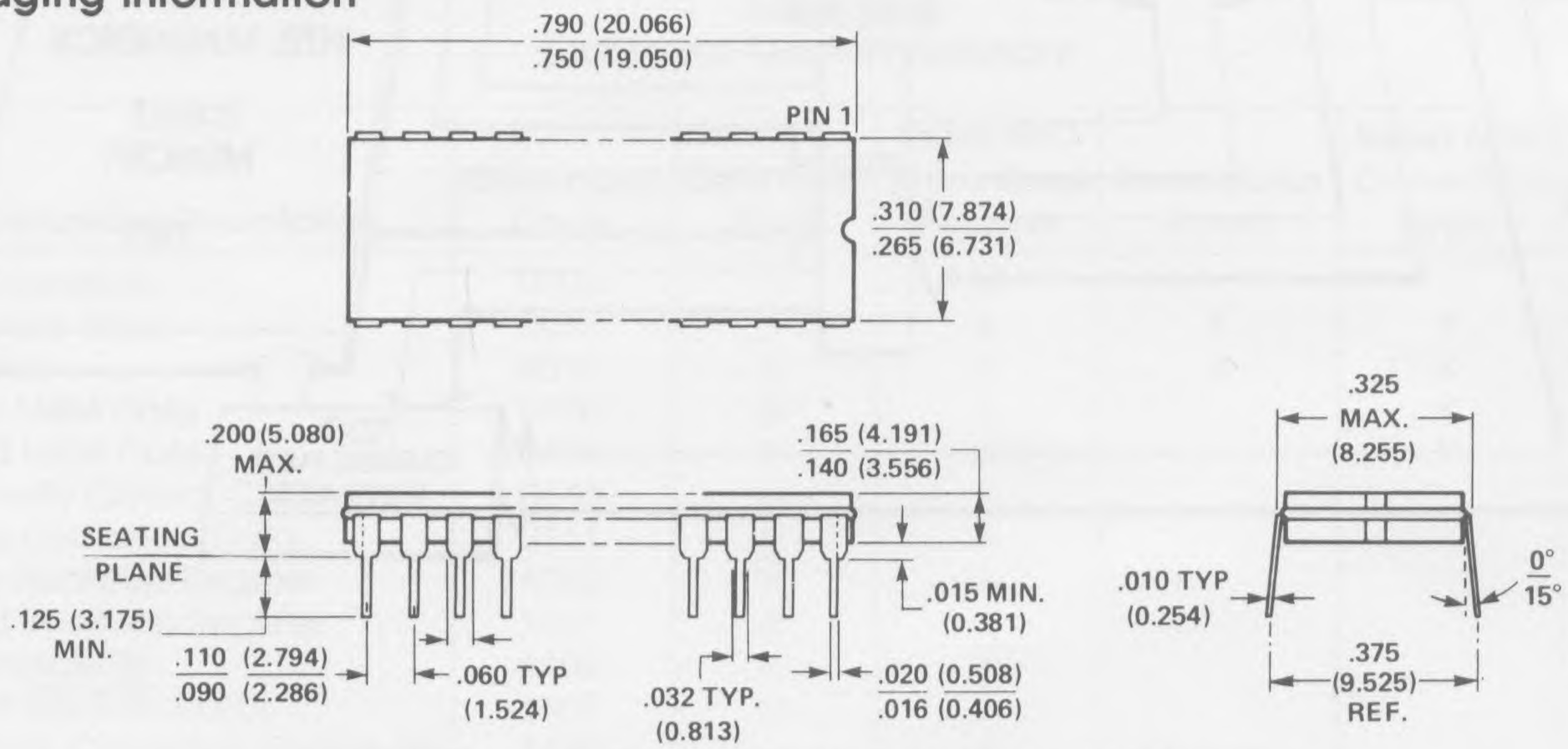
Y+.IN, Y—.IN (Pins 5, 6)

Active low inputs from controller which turn on the high current Y outputs.

Y—.OUT, Y+.OUT, Y+.OUT, Y—.OUT (Pins 9-11 and 7)

High current outputs and their complements for driving the gates of the 7254 VMOS quad transistors which in turn drive the Y coils of the bubble memory.

Packaging Information



16-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD}=12V ± 5%, unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
$\|I_{IN}\|$	Input Current			10	µA	V_I=0.8V
V_{IL}	Low Level Input Voltage			0.8	V	
V_{IH}	High Level Input Voltage	2.2			V	
V_{OL1}	Output Low Voltage			2.0	V	I_{OL}=200mA
V_{OL2}	Output Low Voltage			0.2	V	I_{OL}=10mA
V_{OH1}	Output High Voltage	V_{DD}-2			V	I_{OH}=-200mA
V_{OH2}	Output High Voltage	V_{DD}-0.2			V	I_{OH}=-10mA
I_{OL}	Output Sink Current	200			mA	V_{OL}=2.0V, 30% Duty Cycle
$\|I_{OH}\|$	Output Source Current	200			mA	V_{OH}=V_{DD}-2.0V, 30% Duty Cycle
I_{DD0}	Supply Current			4.5	mA	Chip Deselected: $\overline{CS}$=V_{IH}, V_{DD}=12.6V
I_{DD1}	Supply Current			75	mA	f=100KHz, V_{DD}=12.6V, Outputs Unloaded
I_{DD2}	Supply Current			90	mA	f=200KHz, V_{DD}=12.6V Outputs Unloaded

Capacitance *

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			TBD	pF	

*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f=1MHz, V_{BIAS}=2V, V_{DD}=0V, and T_A=25°C.

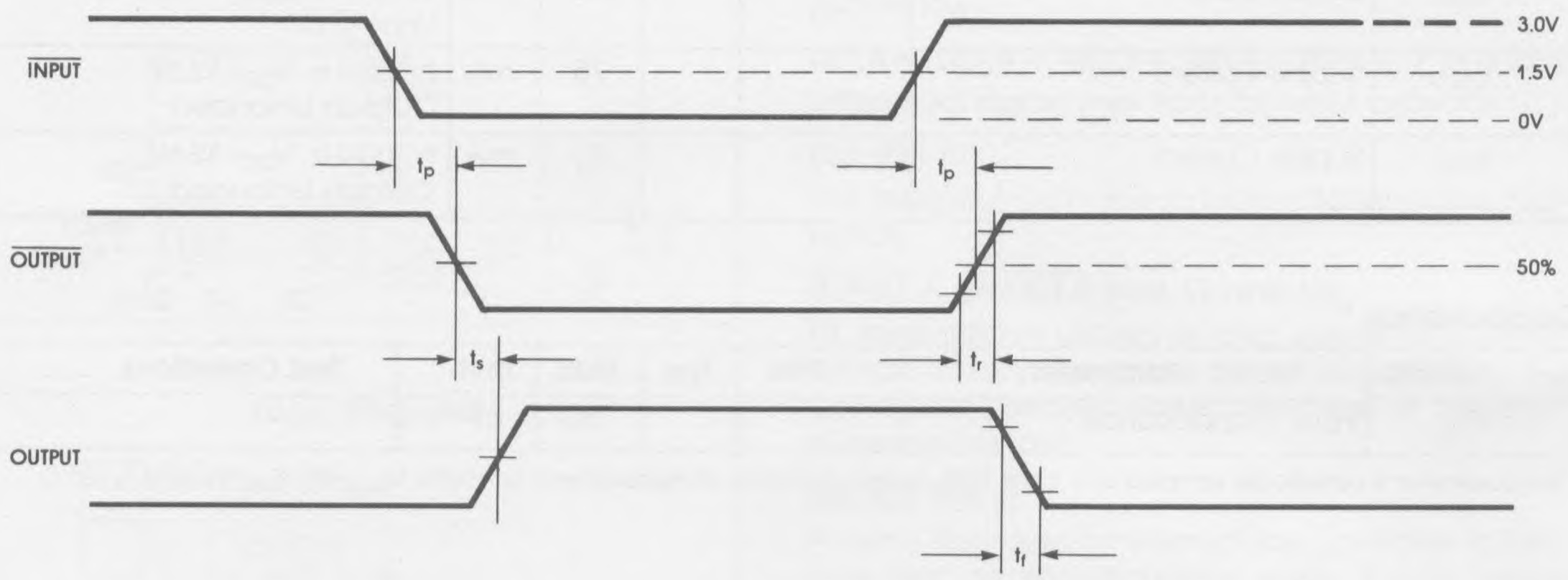
7250

A.C. Characteristics

T_A = 0°C to 70°C, V_{DD}=12V ± 5%, unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{P1}	Propagation Delay from $\overline{X+.IN}$, $\overline{X-.IN}$, $\overline{Y+.IN}$, $\overline{Y-.IN}$			100	ns	500pF Load
t_{P2}	Propagation Delay from $\overline{CS}$ or $\overline{RESET}$			150	ns	500pF Load
t_r	Rise Time (10% to 90%)			30	ns	500pF Load
t_F	Fall Time (90% to 10%)			30	ns	500pF Load
t_S	Skew Between an Output and its Complement			15	ns	

A.C. Test Conditions



Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... -20°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -0.5 to V_{DD} + 0.5V
Supply Voltage, V_{DD} ..... -0.5 to +14V
Output Current 250mA (One Output @100% Duty Cycle)

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

intel® magnetics

Preliminary

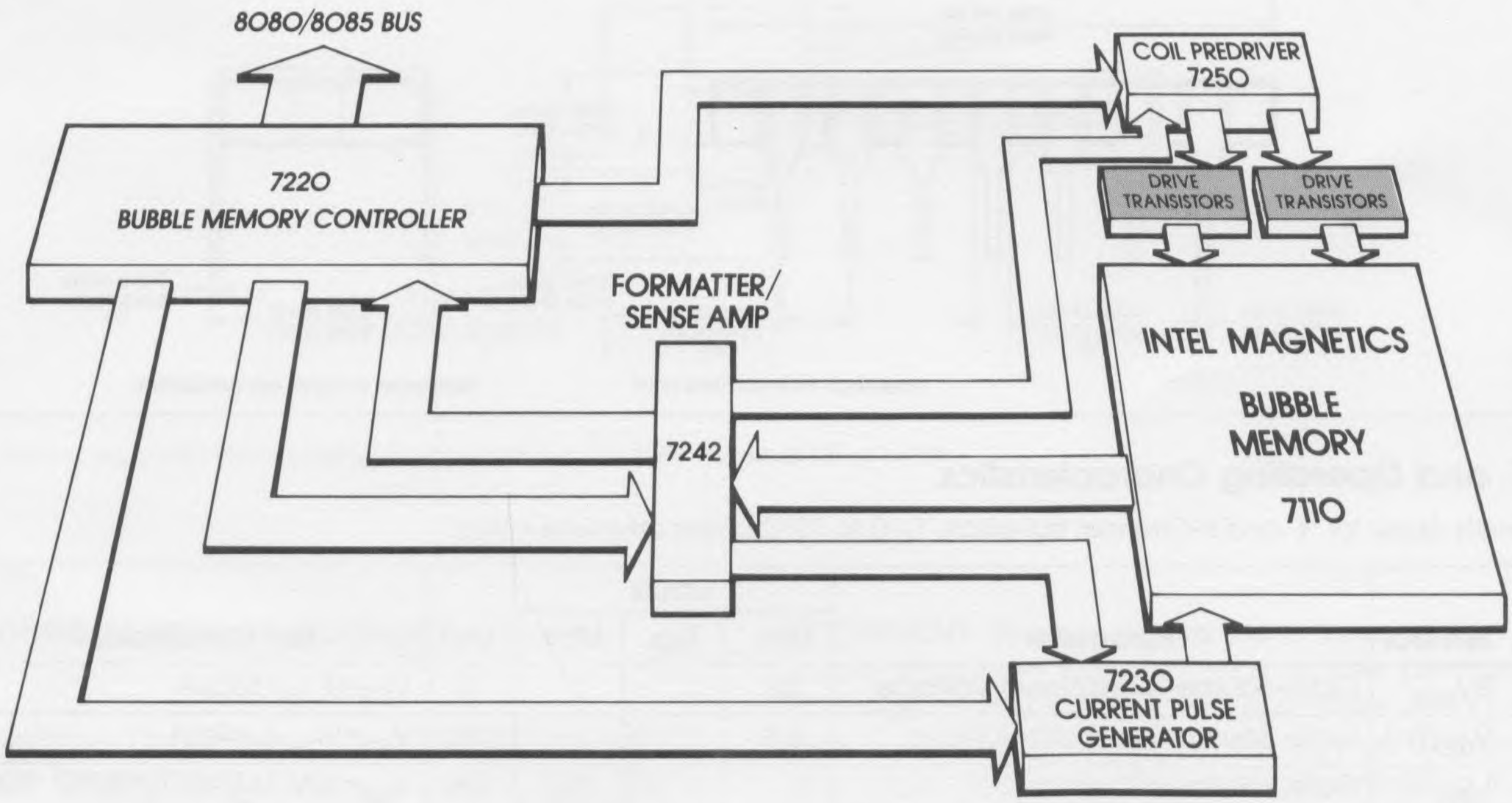
7254
QUAD VMOS DRIVE TRANSISTORS FOR BUBBLE MEMORIES

Features

- **Designed to Drive X and Y Coils of IM's Bubble Memories**
- **No Bias Currents Required**
- **Fast Turn-on and Turn-off — 30ns Maximum**
- **Built-in Diode Commutates Coil Current when Transistor is Turned Off**
- **Operates from V_{DD} Only**
- **VMOS FET Technology**
- **N-Channel and P-Channel Transistors on the Same Chip**
- **Standard 14-Pin Dual-In-Line Package**

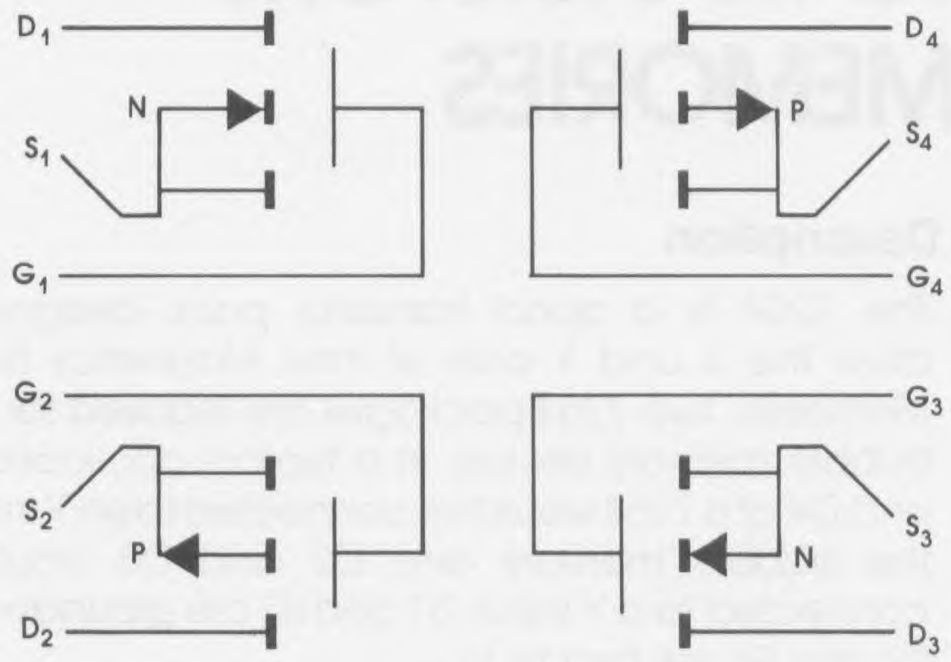
Description

The 7254 is a quad transistor pack designed to drive the X and Y coils of Intel Magnetics Bubble Memories. Two 7254 packages are required for each bubble memory device. In a typical application D1 and D4 of a 7254 would be connected to an X input of the bubble memory and D2 and D3 would be connected to a Y input. S1 and S3 are grounded and S2 and S4 are tied to V_{DD}.



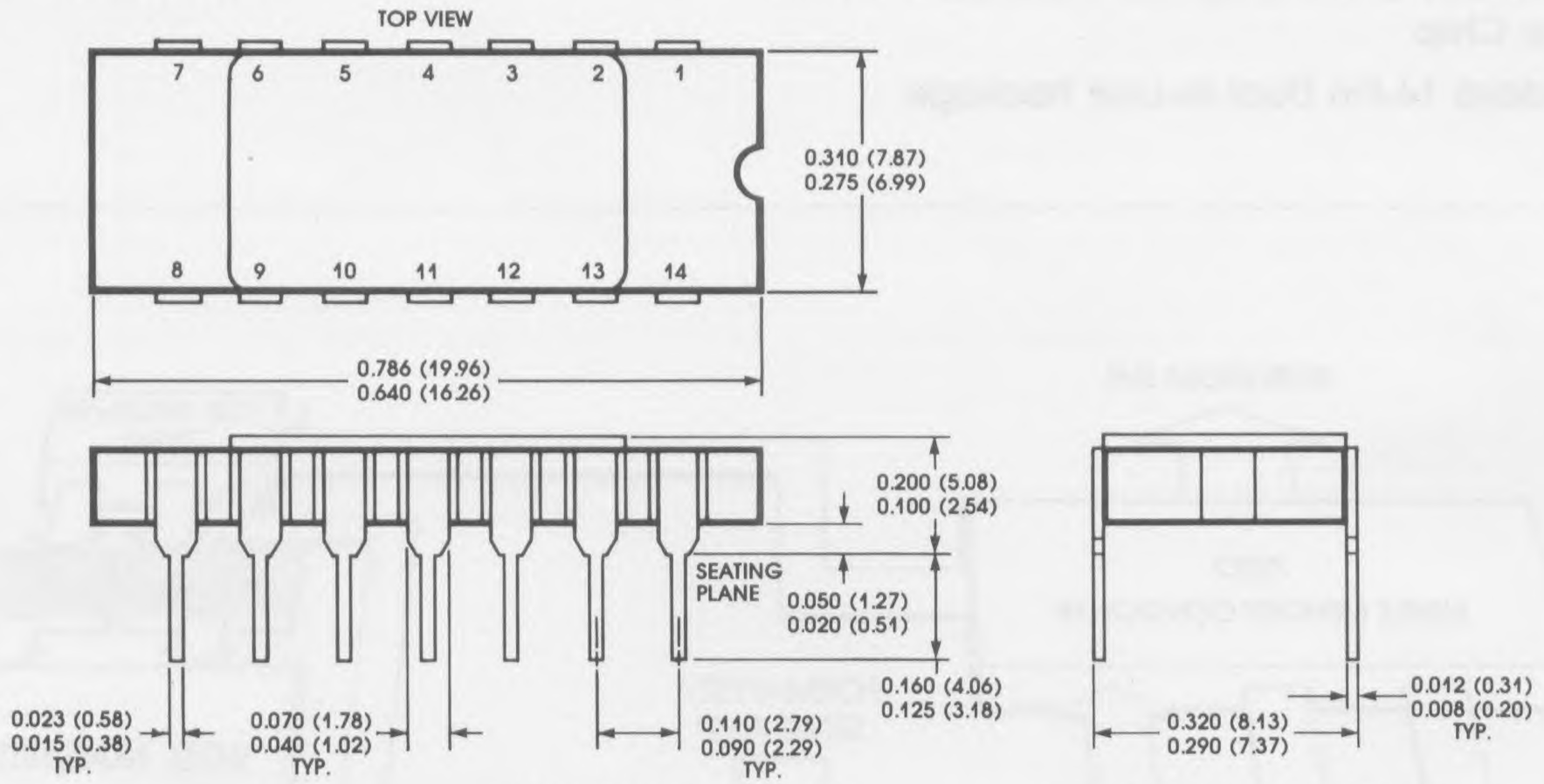
Block Diagram of Single Bubble Memory System — 128K Bytes

Circuit Diagram



Pin Configuration

Packaging Information



TOLERANCE NON-ACCUMULATIVE

DIMENSIONS IN INCHES AND (MILLIMETERS)

D.C. and Operating Characteristics

All Limits Apply for N- and P-Channel transistors, T_A=0 to 70°C unless otherwise noted.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
BV_{DSS}	Drain-Source Breakdown Voltage	30			V	V_{GS}=0, I_D=100µA
$V_{GS}(th)$	Gate-Source Threshold Voltage	0.8			V	V_{GS}=V_{DS}, I_D=1mA
I_{GSS}	Gate Leakage Current			10	µA	V_{GS}=12V, V_{DS}=0, T_A=80°C
I_{DSS}	Drain Leakage Current			500	µA	V_{GS}=0, V_{DS}=24V, T_A=80°C
$r_{DS}(N)$	N-Channel On-Resistance (Note 1)			1.0	Ω	V_{GS}=10V, I_D=1A, T_A=25°C
$r_{DS}(P)$	P-Channel On-Resistance (Note 1)			2.0	Ω	V_{GS}=10V, I_D=1A, T_A=25°C

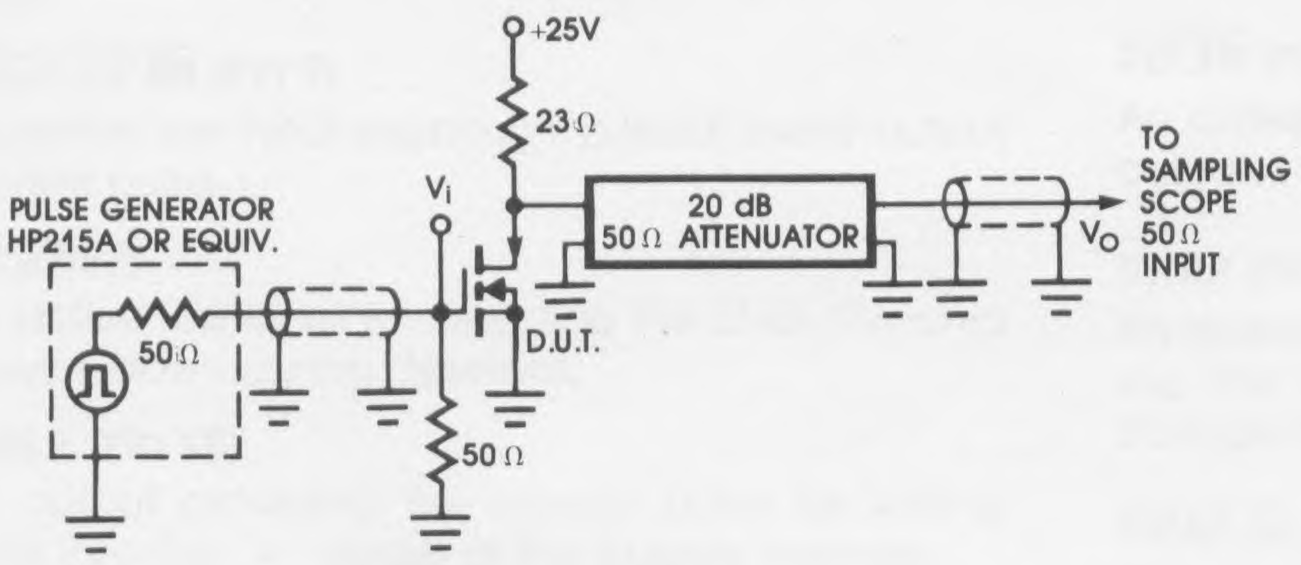
Note: 1. Pulse test — 80µs pulse, 1% duty cycle. r_{DS} increase 0.6%/°C.

7254

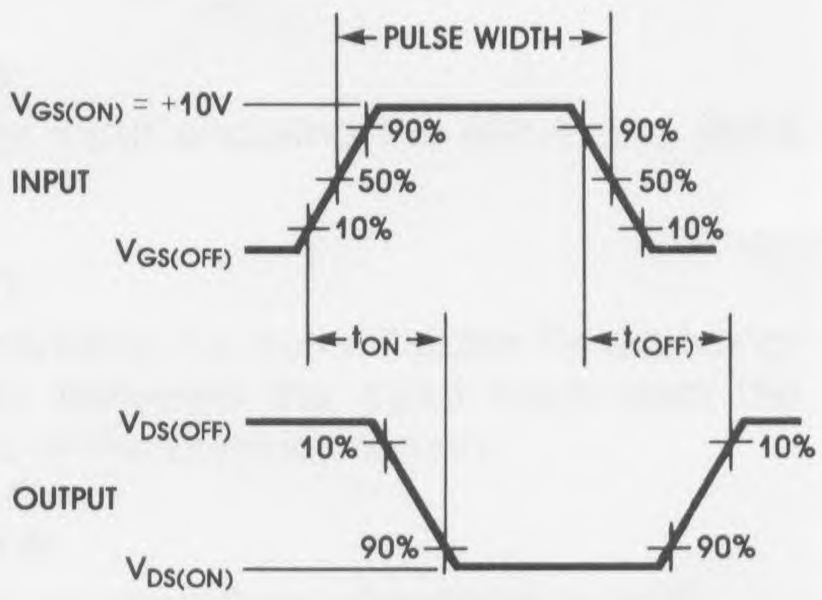
A.C. Characteristics T_A=25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{ON}(N)	N-Channel Turn-On Time			20	ns	See Switching Time Test Circuit and Waveforms below
t_{ON}(P)	P-Channel Turn-On Time			30	ns	
t_{OFF}(N)	N-Channel Turn-Off Time			20	ns	
t_{OFF}(P)	P-Channel Turn-Off Time			30	ns	

Switching Time Test Circuit



Switching Time Test Waveforms



Capacitance T_A=25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}(N)	N-Channel Input Capacitance			175	pF	V_{GS}=0, V_{DS}=12V, f=1MHz
C_{iss}(P)	P-Channel Input Capacitance			190	pF	V_{GS}=0, V_{DS}=12V, f=1MHz

Absolute Maximum Ratings*

Temperature Under Bias ..... -20° to +80°C
Storage Temperature ..... -40° to +150°C
Drain Voltage (with respect to Gate or Source) 30V
Continuous Drain Current 2A
Peak Drain Current 3A
Power Dissipation (T_A=80°C) 1.05W
Power Dissipation (T_A=25°C) 1.75W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

intel magnetics

Preliminary

BPK-71
BUBBLE MEMORY PROTOTYPE KIT

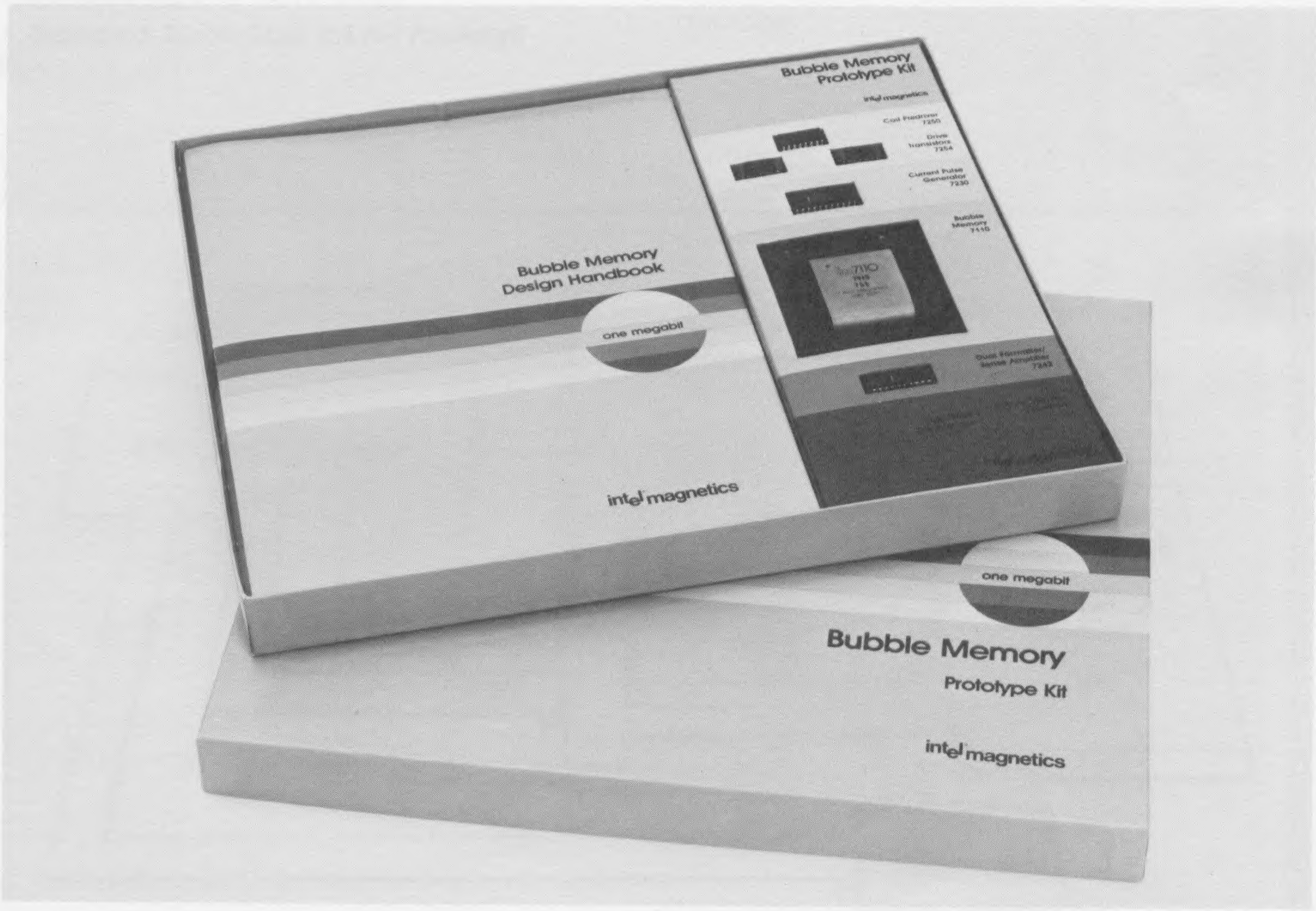
Features

- **Each Bubble Memory Prototype Kit Contains:**
  - **One Intel Magnetics 7110 1 Megabit Bubble Memory**
  - **One 7230 Current Pulse Generator**
  - **One 7242 Dual Formatter/Sense Amplifier**
  - **One 7250 Coil Pre-Driver**
  - **Two 7254 Quad VMOS Drive Transistor Packs**
  - **Complete Documentation for Prototype Systems Including Details for 8085-Based Controller**

Description

Intel Magnetics' 7110 One Megabit Bubble Memories are fully supported with a complete set of LSI interface electronics. The initial Bubble Memory Cell Prototype Kit, BPK-71, enables the user to construct a One Megabit Bubble Memory system with minimum design effort. Application information on system interconnections and a complete description of an 8085-based controller are included in the kit.

The BPK-71 contains all the devices required for a One Megabit Bubble Memory cell.



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Preliminary

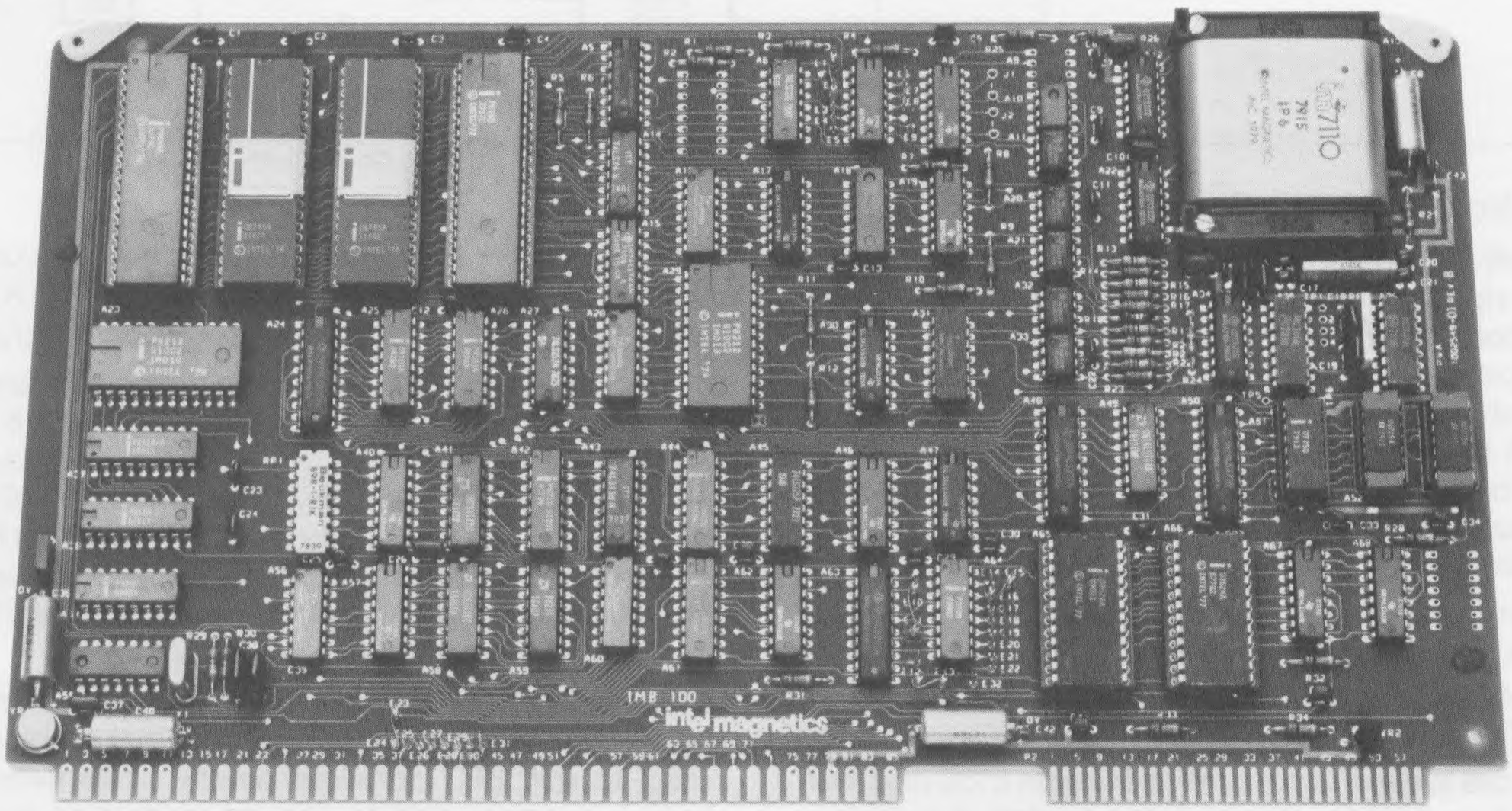
IMB-100
1 MEGA BIT BUBBLE MEMORY DEVELOPMENT BOARD

Features

- **Completely Assembled 1 Mega Bit Bubble Memory Development Board**
- **Standard Intel Interface — 8080/8085 Multibus™**
- **Standard 6.75 x 12-inch SBC Printed Circuit Board**
- **Operates from ±12 and +5 Volt Supplies**
- **Nominal Data Rate 68K Bits/Sec**
- **Average Access Time 40ms**

Description

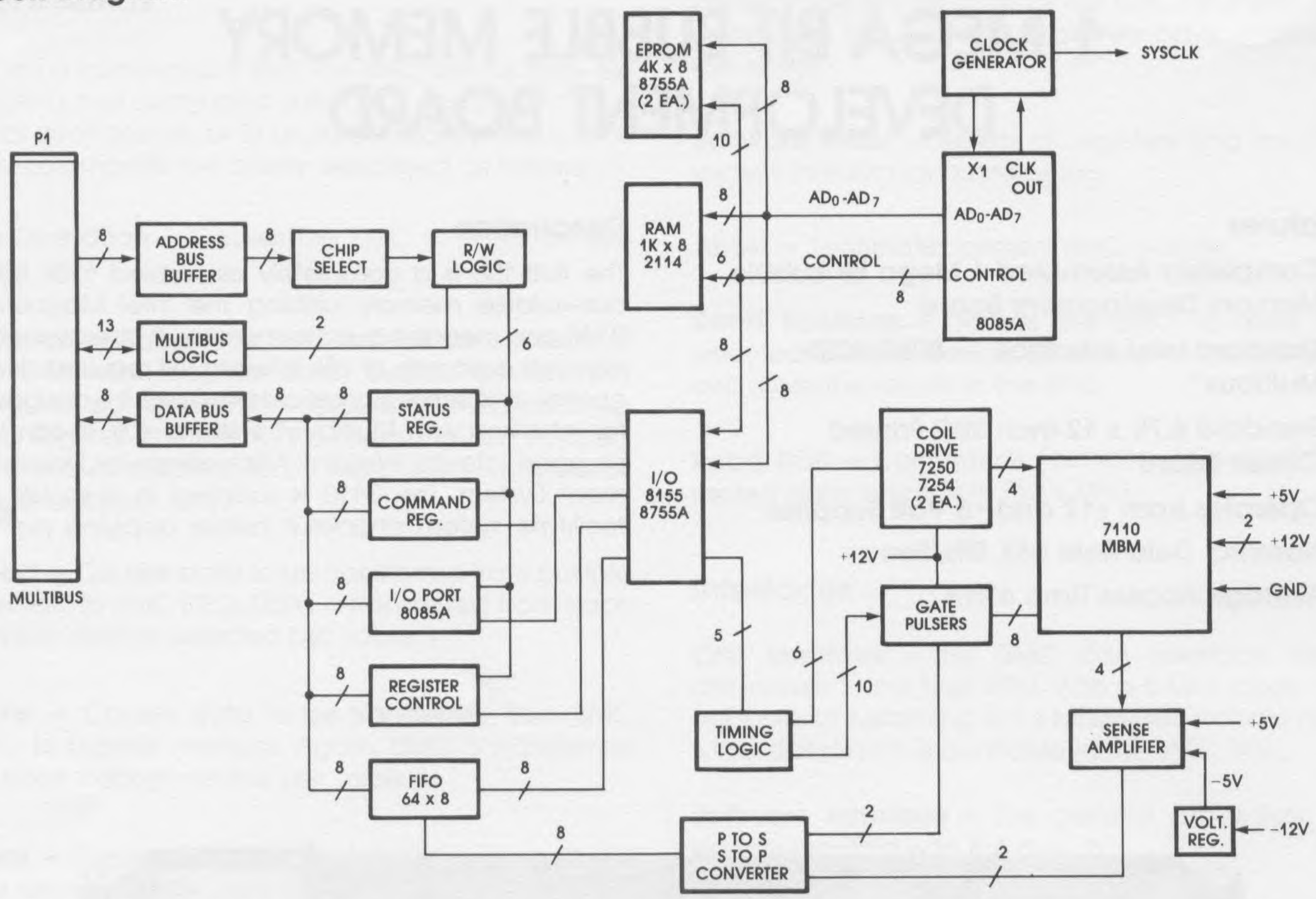
The IMB-100 is a completely assembled 128K byte non-volatile memory utilizing the Intel Magnetics 7110 one megabit bubble memory. It operates at a nominal data rate of 68K bits/sec. All required drive, control, and sense signals are provided. It is designed for interface with Multibus™ systems, e.g. it can be plugged into an Intellec® Microcomputer Development System. The 7110 is supplied in a socket to facilitate system checkout before applying power.



intel magnetics

IMB-100

Block Diagram



Functional Description

The IMB-100 implements a bubble memory controller with standard components. An 8085A with its associated memory and I/O is the heart of the board. The host CPU communicates with the 8085A through a set of registers on the board via I/O commands. The 8085A interprets these registers and controls timing and analog circuits to perform bubble memory accesses. The data is passed via a FIFO on the board (again via I/O commands).

An 8212 latch is used for demultiplexing the internal 8085A bus. One kilobyte of RAM is obtained from two 2114 devices and an 8205 decoder produces chip selects for the RAM and I/O devices.

There are seven I/O ports; three from an 8155 and four from two 8755A's. These ports control the timing generation, status register, host addressable registers, and miscellaneous control bits. The 8755As also contain 2K of EPROM each and the 8155 contains 256 bytes of RAM.

The clock circuit is a crystal controlled oscillator and driver. The board is address decoded by an 8205 decoder. The board address is selected by a jumper option. The board is normally configured to I/O address E0 for data and E1 for command/status.

The registers that are addressable by the host (except command and status) are basically a 16 x 8 RAM whose address can be controlled by either the multibus (through the command register bits 0-2) or the 8085A. The 8085A decides which has access to the registers, since it controls a multiplexer (which provides the address inputs to the RAM). The RAM is provided by two 3101A's.

Bidirectional buffers (in the form of two 8216's) isolate the FIFO from the internal data bus. Shift registers are used to shift FIFO data out serially when writing to bubble memory and to convert serial read data to parallel form. A multiplexer, under control of the 8085A, determines whether the host CPU or the 8085A loads and unloads the FIFO.

Counters that are enabled by the 8085A divide each field rotation into 64 parts. Their outputs are address inputs for two 3624A PROM's. These are programmed

to provide timing pulses to control the analog functions required for the bubble. The outputs of the PROM are latched to provide glitch-free timing signals. The 8085A controls the output of the PROM by controlling the three most significant address bits. Four of the timing signals are converted by the 7250 (coil predriver) into eight 12 volt signals used to drive the 7254 transistor packs. These quad VMOS drivers generate voltage waveforms that create the coil currents in the bubble device.

The current pulses are essentially constant current sinks whose amplitudes are controlled by precision resistors, and whose timing is derived from the PROM-controlled timing. The sense amps are A-C coupled devices.

The IMB-100 is designed to utilize the transparent redundancy inherent in the 7110 magnetic bubble memory device. The bootloop map information of the 7110 is written into the FIFO during system initialization. Gates connected to the FIFO registers gate out the appropriate data to insure that bad loops are not written into and that data from these loops are not read out.

Software Description

A set of programs for exercising the IMB-100 is supplied on double density diskette for use on an Intellec® Microcomputer Development System with ISIS-II. There are six programs which provide for transfers of data between an internal RAM buffer and either a standard ISIS-II device and file or the bubble memory.

The available programs are:

1. INITIALIZE — Initializes Bubble Memory Controller.
2. LOAD EXECUTABLE CODE — The specified ISIS file is expected to be a located object file which is loaded into RAM buffer.
3. RAM TO BUBBLE — Contents of RAM buffer are written into a specified bubble memory file, overwriting existing contents.
4. BUBBLE TO RAM — Contents of specified bubble memory file are read into RAM buffer.
5. DEVICE TO RAM — Specified ISIS file contents are read into RAM buffer.
6. RAM TO DEVICE — Contents of RAM buffer are output to the specified ISIS file.

Specifications

Memory Size

128K bytes.

Interface

All address, data, and control signals are TTL compatible and Intel Multibus™ compatible.

Electrical Characteristics

D.C. Power (Max)

+ 5 Volts d.c. ± 5%,	2.7 A	Max.
+12 Volts d.c. ± 5%,	0.5 A	Max.
−12 Volts d.c. ± 5%,	0.1 A	Max.

Performance

Rotating Field Rate: 50 KHz
Maximum Data Rate: 100K bits/sec
Nominal Data Rate: 68K bits/sec
Average Access Time: 40ms

Connector

86-pin double sided PC edge connector with 0.40 cm (0.156 inch) contact centers.

Mating Connector: Control Data VFB01E43D0A1 or Viking 2VH43/1ANE5

Physical Characteristics

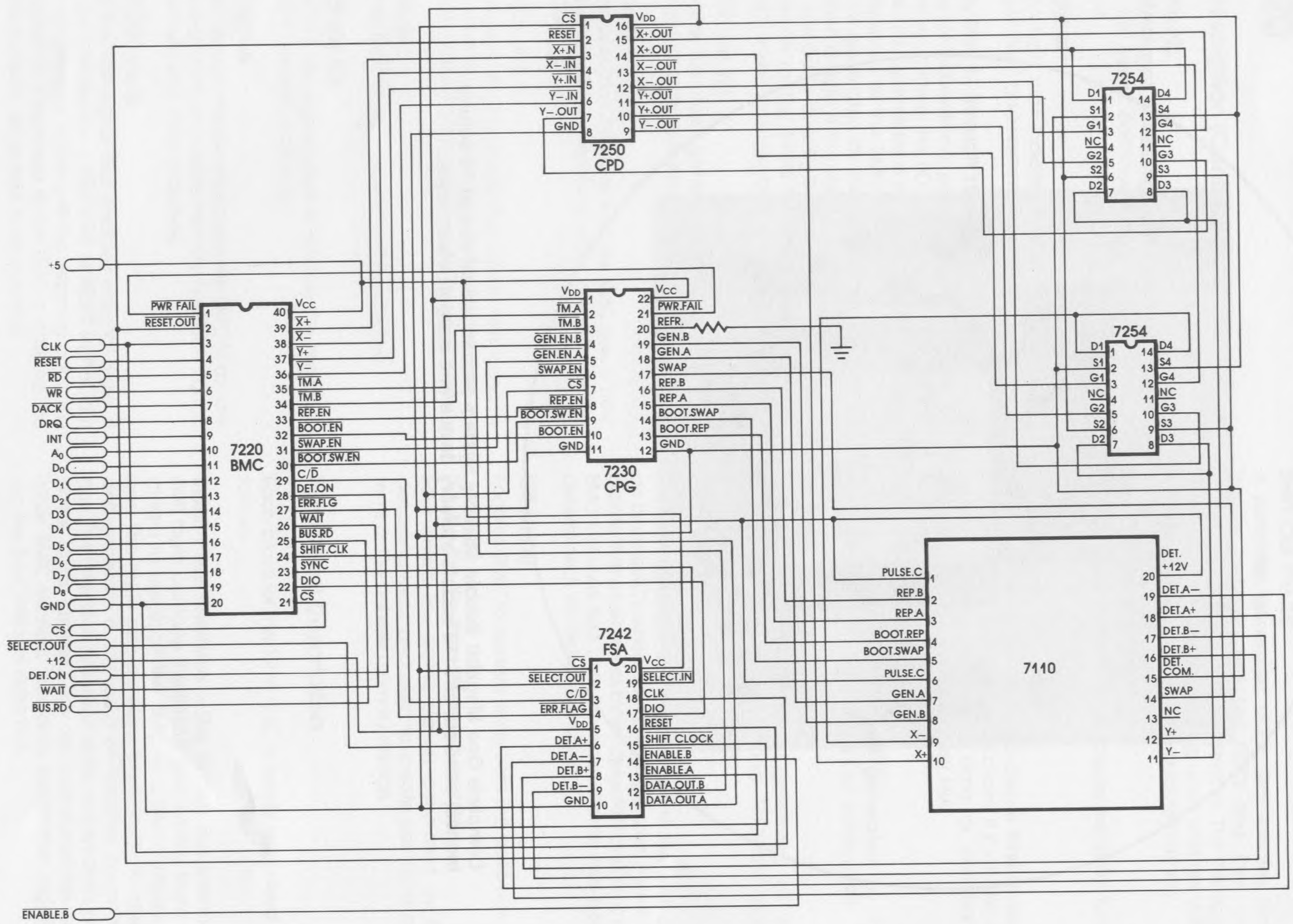
Length: 30.48 cm (12 inches)
Height: 17.15 cm (6.75 inches)
Depth: 1.45 cm (0.57 inch)
Weight: 447 grams (16 ounces)

Environment

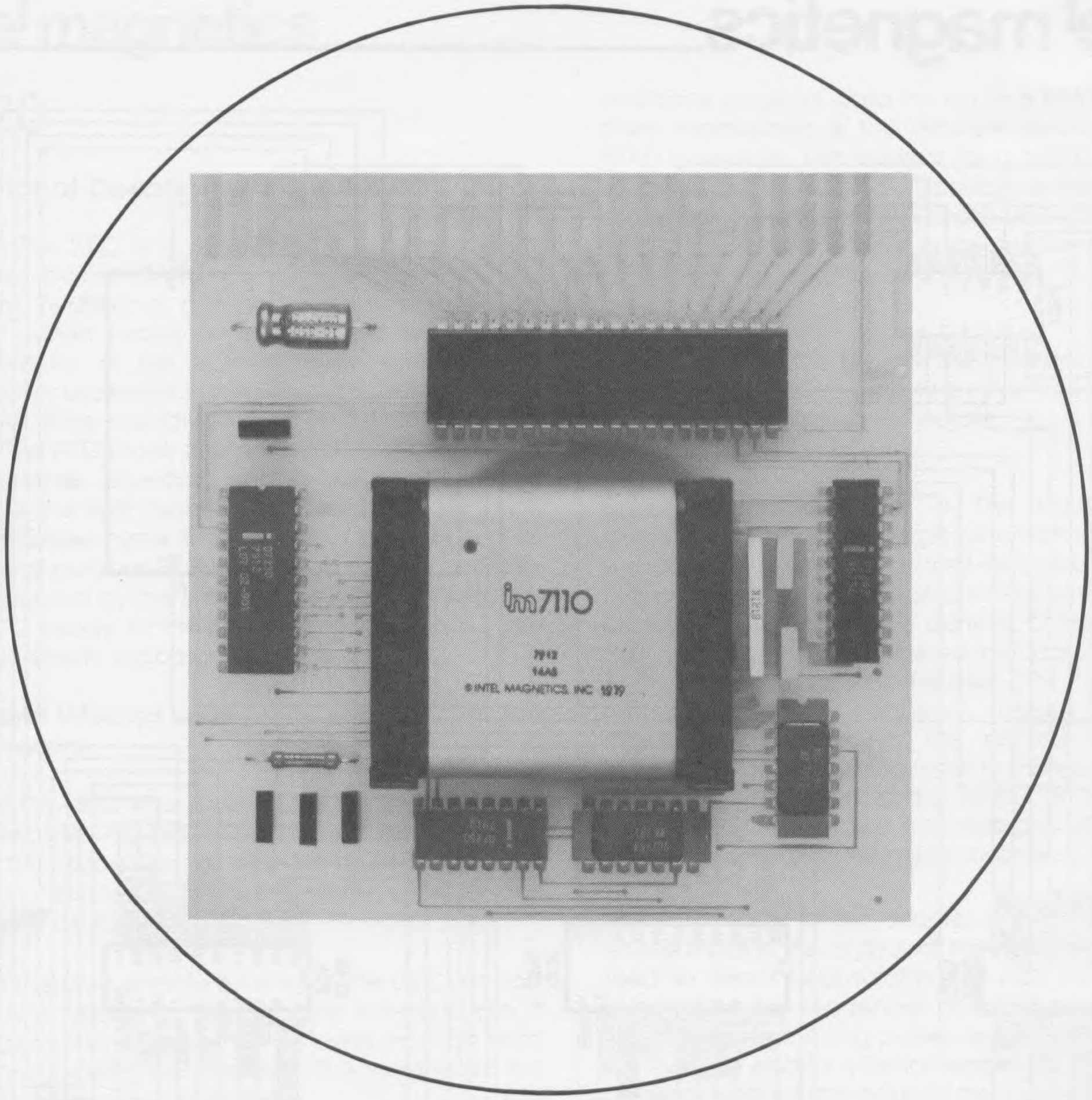
Operating Temperature: 0-50°C

Equipment Supplied

IMB-100	Bubble Memory Development Board
IMB-100	Schematics
IMB-100	Software (double density diskette)



System Interconnect Diagram



Complete One Megabit Bubble Memory System (shown actual size of 16 square inches) consists of 7110 bubble memory device and support electronics:

DESIGN CONSIDERATIONS FOR WORKING WITH BUBBLE MEMORIES

Magnetic bubble memory devices present somewhat of a challenge to the user because they combine low level analog signals (~4 millivolts) with high amplitude current pulses (200-300 mA) and high voltage swings (12V). However, with a little care in the layout of the components, and by following some general design rules, the designer should have no problems in implementing a memory system.

The major features of a good layout for a memory cell are:

1. A ground plane in the area of the bubble detectors and the sense amps.
2. The sense amp is located adjacent to the detector and as close as possible to it. An optional RC filter network is included between the detector and sense amp.
3. The coil drivers are adjacent to the coil connections, away from the detector area.
4. The current pulse generator is adjacent to the majority of the control pins, on the other side of the bubble device.
5. No signal lines should cross the detector to sense amp lines.

General design rules for laying out a bubble memory system include:

1. In general, use both V_{CC} and ground planes if possible. If not, then the power and ground should be gridded (see Intel Memory Design Handbook).
2. Use adequate decoupling capacitors. The CPG and Coil Predrivers both require high current pulses. A high quality ceramic capacitor located adjacent to the power supply pins of each device is recommended. Decouple the detector power supply also.
3. Use wide, short traces for the coil driver outputs. Relatively high (300-400 mA) average currents resonate between coils and the coil power supply. The coil drivers should therefore have both a bulk electrolytic and ceramic decoupling capacitors located close to the drivers.

Power sequencing should not be required if Intel Magnetics support circuits are used. If not, the designer must insure that transients are not created in the coils during power sequencing. Power supplies should be regulated to ±5%.

RECOMMENDED READING

1. A.H. Bobeck and H.E.D. Scovil, "Magnetic Bubbles", Scientific American, June 1971, pp 78-90.
2. A.H. Bobeck, "The Development of Bubble Memory Devices", IEEE ELECTRO 77, April 1977.
3. W. Myers, "Current Developments in Magnetic Bubble Technology", Computer, August 1977, pp 73-82.
4. D. Bryson, D. Clover, D. Lee, "Megabit Bubble Memory Chip Gets Support from LSI Family", Electronics, April 26, 1979, pp 105-111.

Technical articles

Megabit bubble-memory chip gets support from LSI family

Dedicated control and addressing chips, sensors, and driver waveform generators ease system interface problems

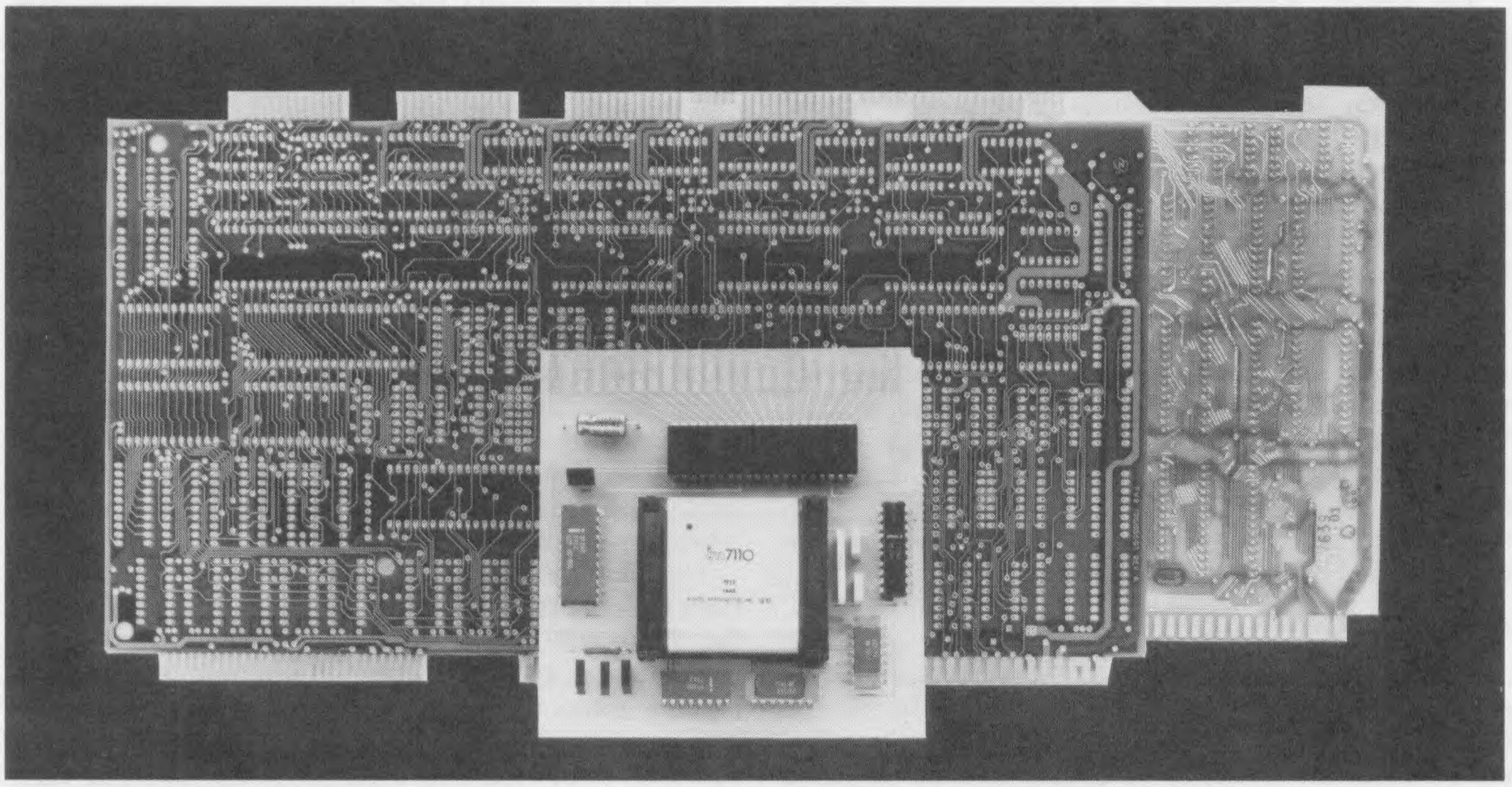
by Don Bryson, Dick Clover, and Dave Lee, *Intel Magnetics Inc., Santa Clara, Calif.*

☐ Because of their potentially high density and nonvolatility, magnetic-bubble memory devices are destined to find diverse applications in areas ranging from low-performance terminals to high-performance mass-storage systems. However, to utilize the attractive capabilities of bubbles, the system designer must deal with an interface problem more challenging than that posed by semiconductor memories.

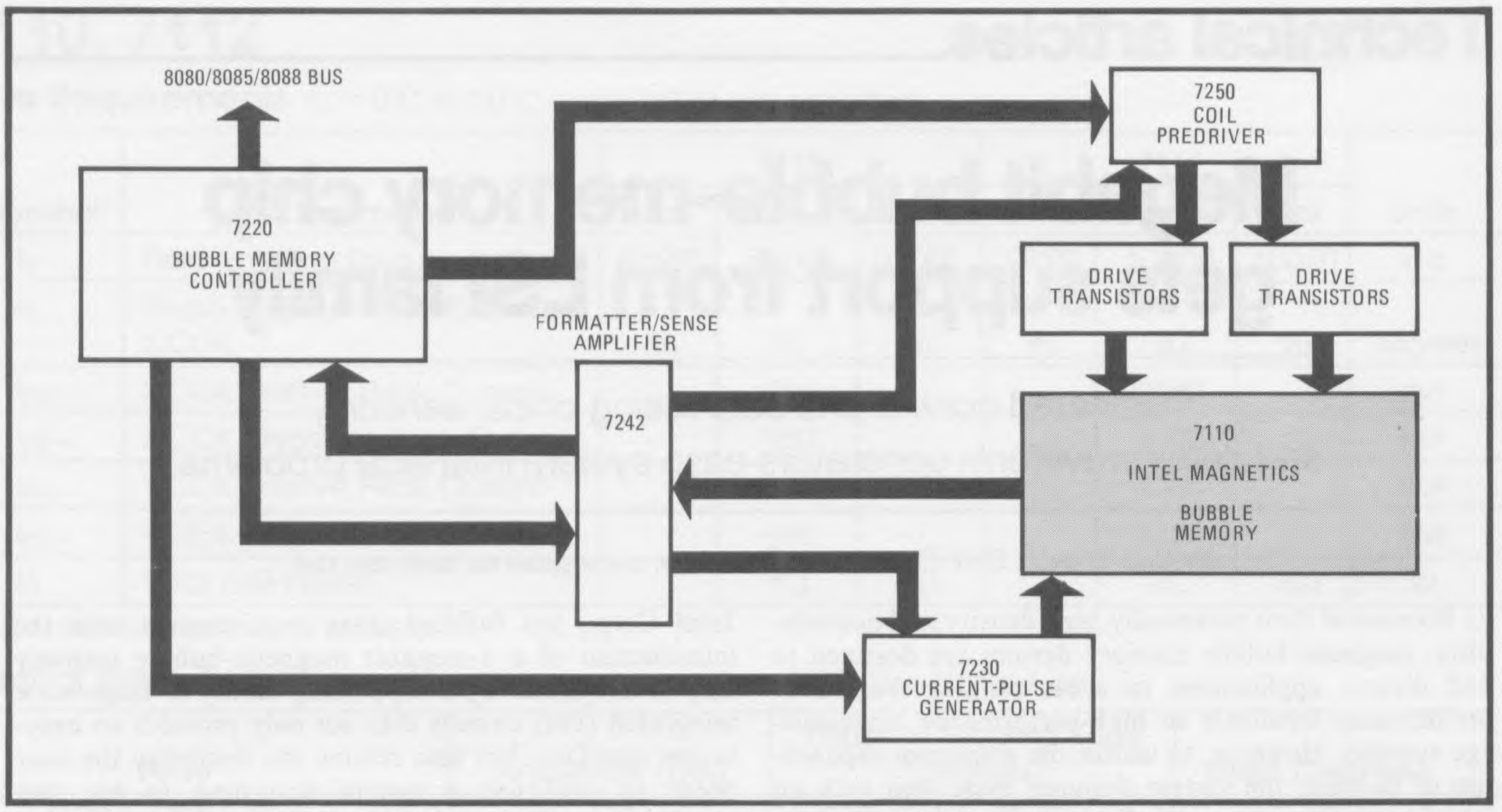
The designer, for example, must not only provide addressing and control logic for the memory device, but also precise current-pulse generation, low-level analog voltage sensing, and relatively high-current waveforms in a set of drive coils. For bubble memories to gain wide acceptance in the marketplace, therefore, their manufacturers must provide more than a memory device. An entire family of parts is needed to ease the designer's complex interface problem.

Now Intel Magnetics, a wholly owned subsidiary of Intel Corp., has fulfilled these requirements with the introduction of a 1-megabit magnetic-bubble memory chip accompanied by a supporting family of large-scale integrated (LSI) circuits that not only provides an easy-to-use interface, but also retains the flexibility the user needs to configure a system according to his own requirements. Figure 1 is a block diagram of the generalized system concept developed by Intel Magnetics. Key ingredients are compatibility with the 8080/8085/8088 bus system, use of advanced LSI technologies, partitioning of control and data paths, and a degree of user programmability. Transparent handling of redundancy, automatic error correction, and power failure reset are built-in features.

Heading the family is the Intel Magnetics 7110, a nonvolatile, solid-state memory with a normal data capacity of 1,048,576 bits. The device includes additional memory that is normally devoted partly to error



Space saver. Availability of Intel Magnetics bubble memory and supporting LSI family of control and driver circuits reduce space, component count for 1-megabit bubble system by order of magnitude, replacing two printed-circuit boards, four 256-K modules, and about 85 ICs.



1. Minimum system. A complete bubble memory system with a storage capacity of 128 kilobytes can be implemented with only one 7110 bubble memory package plus four LSI devices along with two quad transistor packs. The entire system can fit on a 16-square-inch board.

correction and partly to extra storage in the form of redundant loops, to increase the yield of good devices. The accompanying interface circuits are the 7220 bubble memory controller, 7242 formatter/sense amplifier, 7250 coil predriver, and 7230 current-pulse generator. With these, designers can now begin product development using the memory, without concern for drive and interface details. They can treat memory and support electronics as a unique new mass-storage element.

The memory is expected to be used initially in microprocessor applications requiring 128 kilobytes to 2 megabytes of storage. These include terminals, word-processing systems, telecommunications, and process-control wherever nonvolatile storage is required.

The basic components of Fig. 1 can be used to build a minimum system of 128 kilobytes in a 16-square-inch board space. For larger systems, up to eight magnetic-bubble memories (MBMs) can be interfaced with one controller for a megabyte of storage. Through the 7220 bubble memory controller the system interfaces directly with the Intel microprocessor bus systems, so the memory can be treated as a slave to 8080, 8085, 8086, or 8088 host systems. Key functions of the system include binary data organization, standard +12- and +5-volt power supply operation, flexible multiple MBM organizations, single-page (512 bits, or 64 bytes) or multiple-page data transfers, and built-in error correction.

A 1-megabit MBM

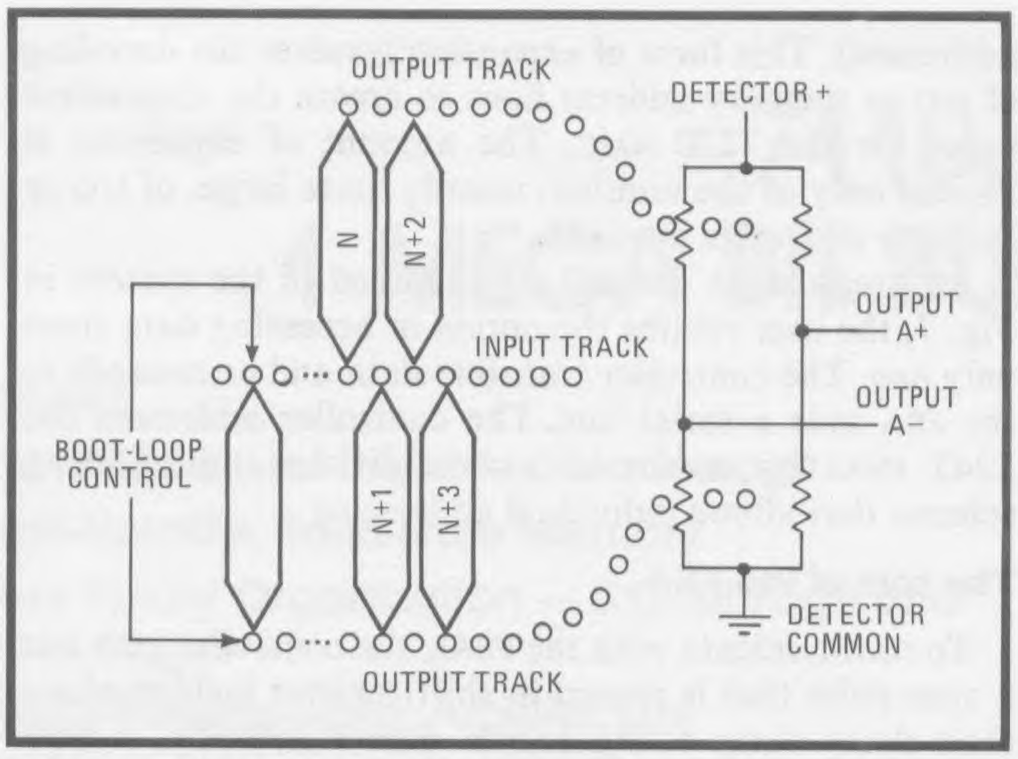
The 7110 is a serial-parallel-serial shift-register storage device with a binary page organization. Its storage elements are cylindrical bubble domains, 2.7 micrometers in diameter, occurring in a thin film of magnetic garnet material grown by liquid-phase epitaxy on a gadolinium-gallium-garnet wafer. After the film is grown, wafer-processing is similar to that used with silicon. Standard photolithography creates conductive and magnetic nickel-iron patterns on the chip. The permalloy patterns form storage loops, input/output tracks, and control elements. The permalloy elements are the usual asymmetrical chevron patterns.

The resulting 2-square-centimeter chip stores 2,048 pages, each holding 512 bits in turn divided into two channels of 256 bits, or 64 bytes. Figure 2 shows one channel of the 7110's basic organization and illustrates the separate block-replicate, block-swap organization. There are 128 data-storage loops per channel divided into two sections of 64 data loops each. A page address is selected and the page is shifted to the starting location for a read or a write operation.

The first part of the read operation nondestructively replicates the bits of the page in parallel on an output track to feed a detector bridge. The bits are shifted serially through the bridge so that the maximum data rate is twice the shift rate. In the write operation, the bits for a new page are first written serially on an input track. Again the maximum data rate is twice the shift rate. The bits shift until they coincide with the bits of the page in storage to be replaced. A swap operation then exchanges the new page for the old at the address location selected.

The performance of the device is readily estimated from the shift rate. The initial product, the Intel Magnetics 7110, will have a shift rate of 50 kilohertz and a storage loop 4,096 bits long. Therefore, the average random access time of a page is about 40 milliseconds. The maximum data rate is twice the shift rate, or 100 kHz. Page read and write times for the 7110 each require a minimum of 327 shift cycles, or 6.5 ms.

From this, the average data rate is 78 kHz (512 bits



2. Organization. Basic bubble memory architecture has a serial-parallel-serial organization. Shown here in simplified form is one of two channels of the 1-megabit MBM. There are altogether 128 loops in each channel, plus a so-called boot loop whose function is to identifiy and keep track of the guaranteed-good loops.

per page divided by 6.5 ms). Most of the reduction from the maximum data rate is associated with the spare storage-loop overhead on the chip. Along with the 256 guaranteed data-storage loops holding the 512-bit pages, there are 64 additional loops. Sixteen of these are guaranteed good so an error-correction code of up to 32 bits can be appended to each 512-bit page. Up to 48 loops can be defective, so that in fabrication a few processing defects do not mean rejection of the chip. Defective loops can be isolated during testing so that they do not interfere with memory operation. Provisions are made in the support electronics to compensate for them. These spare loops, therefore, increase chip yield and hold down costs.

The boot loop

At the system level, the good storage loops and the spare loops must be identified so data is never entered into the spares. To handle this, the bubble memory chip has an additional loop, called the boot loop, that holds a loop-map code for that particular chip along with an index address code. When the system is turned on, the boot code is replicated at the detector. First the index address is located and sets up the address counter in the controller. Then the loop map is read and stored in the Intel 7242 formatter/sense amplifier (FSA). After this, page read or write can begin.

In operation, one page or a burst of pages can be read or written for a given system request. Upon completion, the bubble device itself can be stopped until the next request. This start/stop feature can reduce the average page access time in systems where successive page accesses are not random. Least recently used (LRU) and look-ahead algorithms can be used to put expected future pages at the locations corresponding to the start of the page read or write cycles.

Also at the system level the data rate can be increased by operating bubble devices in parallel. The Intel 7220 controller allows up to eight in parallel. With the 50-kHz 7110, the average bit rate then becomes 625 kHz. With two controllers and 16 7110s, the bit rate is 1.25 MHz.

TABLE 1: BUBBLE MEMORY SYSTEM PERFORMANCE

	One magnetic-bubble memory cell (MBM)	Four MBMs	Eight MBMs operated in parallel	Eight MBMs multiplexed one at a time
Capacity	128 kilobytes	512 kilobytes	1 megabyte	1 megabyte
Average data rate	62.5 kHz to 125 kHz	250 kHz to 500 kHz	500 kHz to 1 MHz	62.5 kHz to 125 kHz
Average access time	50 to 25 ms	50 to 25 ms	50 to 25 ms	50 to 25 ms
Power dissipation (100% duty factor)	6 W	20 W	40 W	11 W
Standby power	1.3 W	3.7 W	7.0 W	7.0 W
Board area	16 in.^{2}	45 in.^{2}	90 in.^{2}	90 in.^{2}

Sometime in the future a 100-kHz MBM, the 7112, will be offered with twice the data rate. Table 1 shows the range of expected performance characteristics encompassed by the 7110 and 7112.

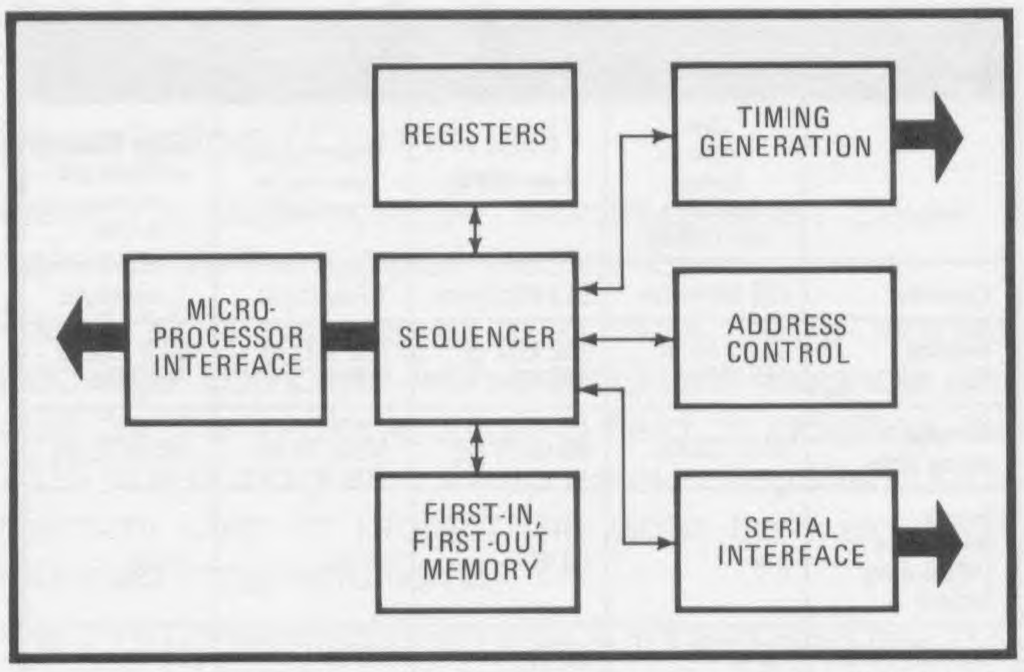
Support components

The user interface is provided by the Intel 7220 bubble memory controller (BMC). The controller is a 40-pin LSI device implemented in Intel's HMOS technology. Figure 3 is a block diagram of the 7220 BMC. Major functions of the controller are to provide the bus interface, to generate all memory system timing and control functions, to maintain memory address information, and to interpret and execute user requests for data transfers.

The heart of the bubble system is the 7242 formatter/sense amplifier diagrammed in Fig. 4. The FSA is a dual-channel device that can interface directly with both channels of the memory. Three key functions of the 7242 are sensing the low-level bubble signals, handling the redundant loops, and buffering data. In addition, the user may choose a circuit for detecting and correcting burst errors. The 7242 FSA communicates with the 7220 BMC via a serial bus, so that a 20-pin DIP may be utilized. The operation of the FSA is discussed in more detail later. An advanced n-MOS technology was chosen to incorporate sensing and data-handling functions.

A Schottky bipolar process was chosen to implement the Intel 7230 current pulse-generator (CPG) because of the relatively high peak currents required. The 7230 CPG interfaces directly with the 7220 BMC and the bubble memory device and provides the fast, high-current pulses required by the latter. It consists of a reference-current generator, a power-failure-sensing circuit, and 12 current sinks switched on or off by the 7220 controller. The chip contains a power-down circuit that shuts off the current sources whenever the chip is disabled. The 22-pin device's logic diagram is shown in Fig. 5.

Finally, the support electronics makes it possible to drive the coils of the bubble memory. The peak currents required in the coil are beyond the capacity of standard IC devices, so a coil predriver (CPD) that interfaces the 7220 controller and discrete transistors has been developed. The Intel 7250 CPD is a C-MOS device in a 16-pin DIP that translates the TTL outputs of the 7220 controller into high-voltage, high-current signals that can be used



3. User interface. The 7220 controller is a complex LSI 40-pin device that provides the interface to the system bus, generates all memory system timing and control functions, and supervises the execution of data transfer requests.

to drive transistors. The logic diagram of the 7250 is shown in Fig. 6. Quad transistor packs are used to drive each coil. V-channel MOS field-effect transistors are preferred for the drivers, since they are fast, require no bias currents, and have a built-in diode to commutate the coil current when the transistor is turned off. However, the 7250 CPD has the ability to provide up to 200 milliamperes of base current for bipolar drivers.

System features

Since the system designer is given a complete set of LSI parts, he can concentrate on higher-level system objectives, instead of having to learn the intimate details of bubble memory interfacing. He saves still more time by working with a standard bus already familiar to him, rather than designing counter circuits and trying to convert millivolt signals into TTL voltage levels. The system operates from +12 V and +5 V only, with circuitry to monitor these voltages. Should the voltages drop below acceptable levels, it will shut itself down in an orderly manner, so that integrity is preserved.

Even though the details of interfacing to the bubble device are hidden, the support electronics are flexible enough to accommodate widely different system designs. Figure 1 shows the minimum system—that is, it contains only one bubble device (128 kilobytes) and the required support electronics. Figure 7 is a block diagram of a larger system containing eight bubble memory cells. Each contains a bubble device, a 7230 CPG, a 7250 CPD, and two quad transistor packages. A single 7220 BMC can directly control from one to eight bubble memories.

Expansion to larger systems can be accomplished in two ways. In the first approach, provisions are made in the BMCs for paralleling controllers. This provides greater word width at the bus, and each controller can still accommodate from one to eight bubble memory devices. In the second, each support device has a chip-select pin so that banks of devices can be switched into or out of the circuit under external control. The maximum number of devices in each bank remains eight. In addition to these two expansion modes, the 7220 BMC also has a chip-select input so that entire subsystems may be multiplexed (or, more typically, located at different I/O addresses). This form of expansion involves the decoding of I/O or memory-address lines to create the chip-select input for the 7220 BMC. The amount of expansion is limited only to the number, usually quite large, of I/O or memory addresses available.

Although eight devices are included in the system in Fig. 7, the user retains the option of accessing data from only one. The controller transfers data and commands to the FSA over a serial bus. The controller addresses the 7242 FSAs by means of a time-division multiplexing scheme that allows individual addressing.

The role of the FSA

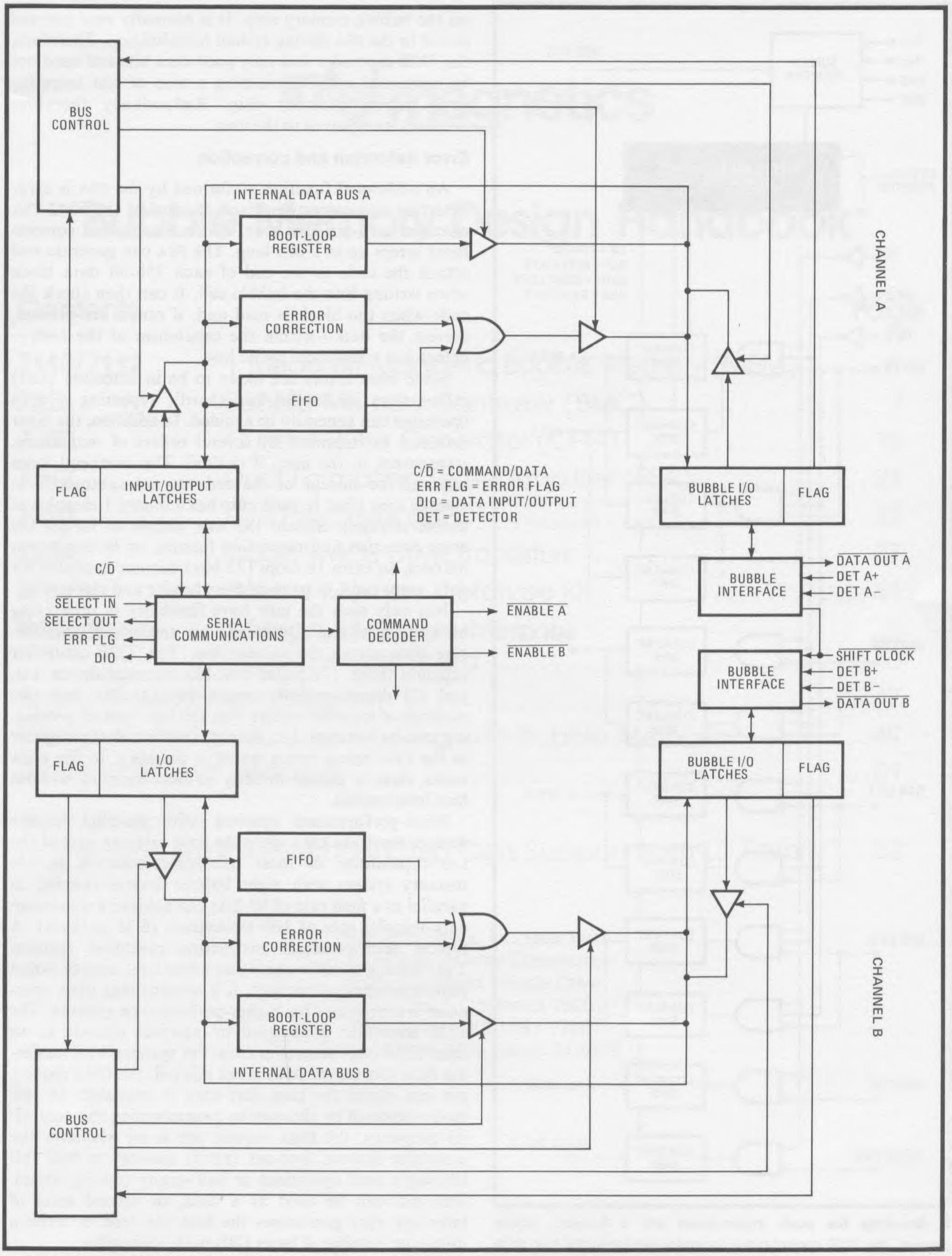
To communicate with the FSAs, the controller puts out a sync pulse that is passed in shift-register fashion along their daisy-chain configuration. Simultaneously, a data stream is put out on the serial bus. As each FSA receives its sync pulse, it examines the serial bus to determine whether it is being addressed. Note that each channel of the dual FSA can be individually addressed since the sync is passed internally from channel A to channel B. Commands are distinguished from data by a C/D pin controlled by 7220 BMC. The direction of data on the bus is determined by the mode the FSA has been set to by the controller. However, FSAs are forced to "listen" to the serial bus when a logic C/D line occurs.

Any FSA that is not addressed during a command automatically disables and removes itself from the bus. This action provides an added benefit, in that each FSA channel also has an enable output active only when selected. It is connected to the chip-select pins of the other support circuits, so each bubble memory device that is not needed for the present access remains powered down. The only restriction on the selection of devices to be accessed is that the number of channels to be accessed be binary (i.e., 1, 2, 4, 8, or 16) and that each multiple group be contiguous in the FSA daisy chain. For example, if the user's data rate requires that two bubble devices be accessed simultaneously, the two must be either devices 1 and 2 or 3 and 4, etc.

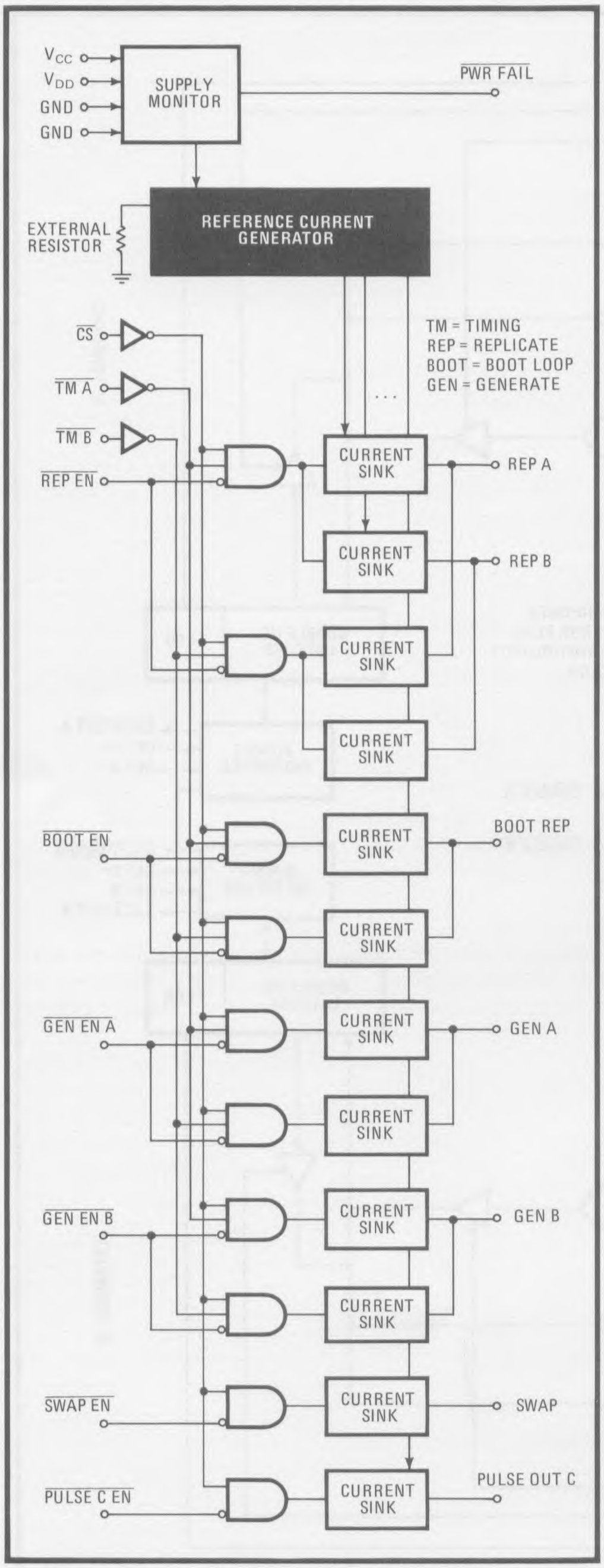
In any configuration, data is transferred in serial form and reassembled into an 8-bit byte by the 7220 controller. The serial bus operates at a minimum rate equal to 20 times the rotating field rate so that a bit of data can be transferred to or from each FSA channel during each field rotation. Thus a system containing a megabyte of bubble memory can be useful in low-data-rate, low-power systems as well as in high-performance systems. The partitioning of most of the data handling into the FSAs makes this flexibility possible.

It now becomes readily apparent why the FSA is considered the heart of the system: it enables the system to parallel as well as multiplex memory devices easily—something not possible previously with bubbles. All this is accomplished with minimum parts since the sense amplifier and redundancy handling are in the same package. Redundancy handling involves deleting bits read from defective loops on the bubble chip and inserting zeros into the data stream when writing to the bubble chip. This function is ideally performed by the FSA as the defective loops are different in each bubble device.

A map of defective loops is contained in the boot loop



4. Heart of the matter. The 7242 dual formatter/sense amplifier (FSA), implemented with an advanced n-MOS process, makes available many system functions that are required by the user, but handles them transparently. Besides permitting optional error correction and detection, the FSA makes it possible for the memory devices to be paralleled and multiplexed with minimum parts count.



5. Reaching the peak. Implemented with a Schottky bipolar process, the 7230 current-pulse generator produces the high peak currents required to power the 7110 MBM. It incorporates a power-failure-sensing circuit and a power-down circuit that shuts off the current sources when the chip is disabled.

on the bubble memory chip. It is normally read out and stored in the FSA during system initialization. Therefore, the 7220 controller sees only good data bits and need not be concerned with maintaining a map of bad loops for each bubble memory chip. Redundancy therefore becomes transparent to the user.

Error detection and correction

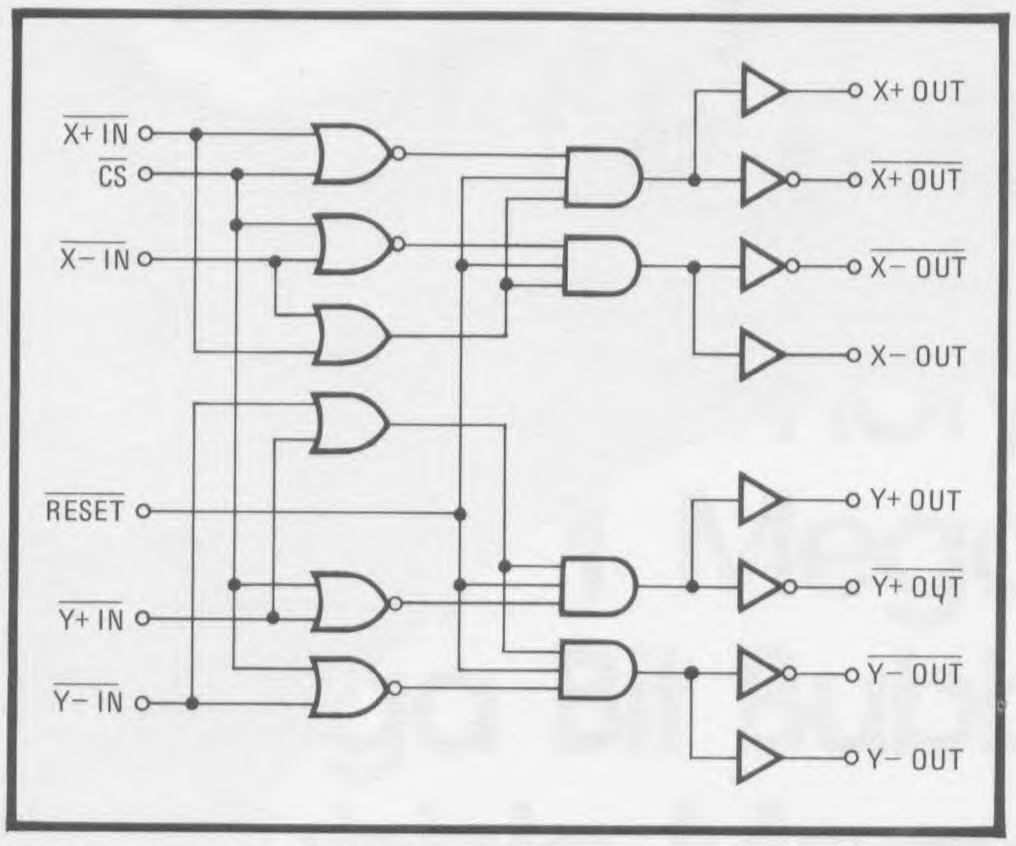
An additional function performed by the FSA is error detection and correction. Each channel of the 7242 FSA contains a 14-bit Fire code, which detects and corrects burst errors up to 5 bits long. The FSA can generate and attach the code to the end of each 256-bit data block when writing into the bubble cell. It can then check the code when the block is read and, if errors are present, correct the data—within the capabilites of the code—before it is transferred to the host.

Since most errors are likely to be in detection (soft) rather than in bubble loss (hard), repeating a read operation can generally be avoided. In addition, the error rate can be improved by several orders of magnitude, transparent to the user, if desired. The overhead loops required for storage of the code do not subtract from storage area (that is, each chip has a binary 1 megabit of usable storage). Should the user decide to forego the error detection and correction feature, or to implement his own, an extra 16 loops (32 bits) become available for data, error code, or page-address header and storage.

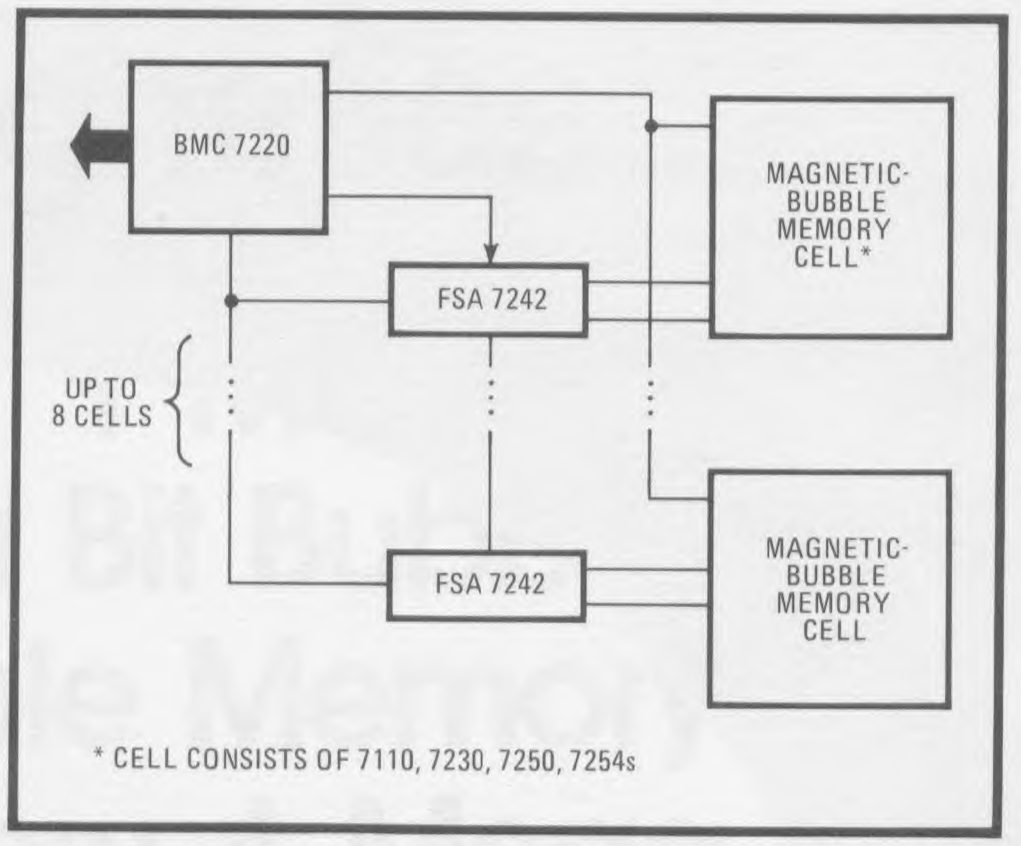
Not only does the user have flexibility in organizing his system, he can also choose his methods of transferring data across the system bus. The 7220 controller supports three: (1) polled I/O, (2) interrupt-driven I/O, and (3) direct memory access (DMA). The first two methods of transfer require that the host central processing unit be involved, i.e., data is transferred to a register in the CPU before being stored in memory. In the DMA mode, data is passed directly to host memory without host intervention.

High-performance systems with parallel bubble devices must use DMA since the data rate can exceed the I/O capabilities of most microprocessors. A bubble memory system with eight bubble devices running in parallel at a field rate of 80-kHz can achieve a maximum data-transfer rate of 160 kilobytes/s (6.25 μs/byte). A typical microprocessor instruction execution requires 2 μs. Since a transfer execution under CPU control would require several instructions, it is obvious that DMA operation is a necessity for higher-performance systems. The 7220 controller is designed to interface directly to an Intel 8257 DMA controller chip. For systems with moderate data rate where DMA is not desired, the DMA request pin can signal the host that data is available. In this mode (selected by the user by programming the controller properly), the DMA request pin is set whenever the controller first-in, first-out (FIFO) memory is half full (during a read operation) or half empty (during write). This pin can be used as a data, or second level of interrupt, that guarantees the host can read or write a minimum number of bytes (20) to the controller.

The last, and lowest, performance mode is provided by a status bit in the controller that indicates presence of data in the FIFO. The host could continually poll status



6. Predriver. The 7250 converts TTL outputs of the 7220 controller into the high-voltage, high-current waveforms used to energize the transistors that drive the coils of the MBM through quad transistor packs. The coil predriver can interface with either V-MOS FET drivers or can provide up to 200 mA of base current for bipolar types.



7. Big system. This system diagram shows how the 7220 bubble-memory controller can be used to control up to eight bubble memory cells for a total capacity of 1 megabyte. Even more capacity can be attained by paralleling extra controllers. Additionally, the 7220's chip select input permits multiplexing entire subsystems.

and output data when the FIFO is available, but this mode is useful only in the lowest performance system.

After power-up, the host must initialize the system. Communication with the controller is accomplished via a set of addressable registers contained within the controller. These registers are addressed by the host and written with information relating to the desired operating modes (for example, DMA is enabled, the number of data blocks is specified, etc.). The host must then issue a command to initialize. The controller proceeds to read the bootstrap loop of each bubble device (which is redundantly coded) and write the bad loop information into the bootstrap loop register contained in the corresponding FSA. The controller begins with the first FSA in the chain and continues down the chain in order until all devices have been initialized. Each bubble device is left in the home position (page 0 is ready to be read).

Sequence of events

After initialization, the controller, if enabled, interrupts the host and is ready for data transfers. The host writes an address into the controller registers, issuing a read or write command. The controller then takes over and accesses the desired page or pages of information. An interrupt is normally issued upon completion, but it may be inhibited by the user. An address is maintained and updated for each bubble device in the system, regardless of organization, within the controller. If a block transfer overflows the address boundary of a bubble device or devices, the controller will automatically switch to the next in the chain. A maximum of 2,048 pages of data can be transferred with a single-command sequence. Should a power-down occur during a transfer, the controller will automatically shut down the coil drivers in the proper sequence, if power remains at acceptable levels for about 100 microseconds.

The user requests data transfers by addressing a command/status register in the 7220 BMC. A large number of commands are available to the user, including several that are useful for system diagnostics.

The most commonly used commands are:

- Initialize—performed after power-up in order to reset the system.
- Read—causes the selected pages of bubble memory to be accessed.
- Write—writes user data into selected pages of the bubble memory.

Read and write can be specified for 1 to 2,048 pages. In addition, a seek command lets the user predict his next read address, avoiding additional latency. However, in multiple-page read or write operations, consecutive page addresses are physically located so the next page is available immediately upon completion of the preceding operations. Additional commands include reading and writing of the bootstrap loop registers in the FSAs, or the bootstrap on the bubble chip, a software reset, and an abort command. Status bits provided to the user include a busy signal, an operation complete flag, a FIFO ready flag, and several error flags, including timing and correctable and uncorrectable error. Status of each FSA can be determined by the host processor with a special command. Interrupt masking lets the user decide whether he is interrupted by errors or by normal operation-complete interrupts. The combination of error-correction capability, a versatile command set, and appropriate status flags also lets him perform on-line maintenance checks to enhance reliability.

The key design features incorporated in the Intel Magnetics MBM systems approach were chosen after a strong effort to define the appropriate markets for bubbles. Ideas from more than 200 potential customers were gathered and greatly influenced the choices of size, speed, and organization. Thus, two years after inception, the program will yield bubble memory products including development boards so customers can begin evaluating the 1-megabit bubble memory product line. □